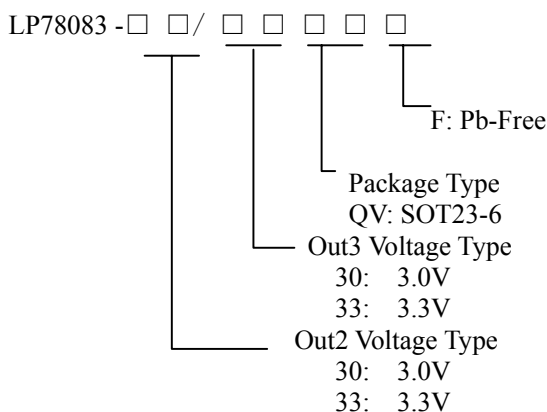


650mA High Efficiency Synchronous Buck with Dual Channel LDO

General Description

The LP78083 are PMU, and contain a 650mA Buck DC/DC and dual channel 350mA Linear Regulator, Buck DC/DC is a constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency. The 2.1V to 6.5V input voltage range makes the LP78083 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy-terminals. Internal synchronous rectifier with low RDS(ON) dramatically reduces conduction loss at PWM mode. The internal synchronous switch increases efficiency while eliminate the need for an external Schottky diode. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small 2*2 DFN-8 package provide small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Ordering Information



Features

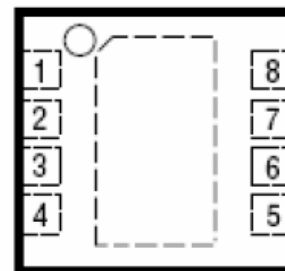
- ◇ 650mA Buck High Efficiency: 96%
- ◇ 1.5MHz Fixed-Frequency PWM Operation
- ◇ Adjustable Output From 0.6V to VIN
- ◇ 350mA LDO: 3.0V and 3.3V Fixed output
- ◇ 100% Duty Cycle Low Dropout Operation
- ◇ Available in 2*2 TDFN-8 Package
- ◇ Low than 1µA Shutdown Current

Applications

- ◇ Portable Media Players/MP3 players
- ◇ Cellular and Smart mobile phone
- ◇ PDA
- ◇ DSC
- ◇ Wireless Card

Pin Configurations

TOP VIEW



PIN NO	Function
1	SW
2	GND
3	OUT2
4	VIN
5	OUT3
6	EN
7	VDD
8	FB1

Marking Information

Please see website.

Typical Application Circuit

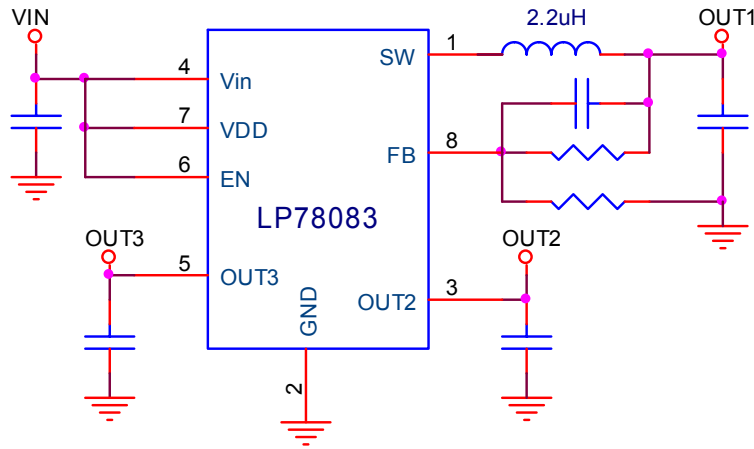
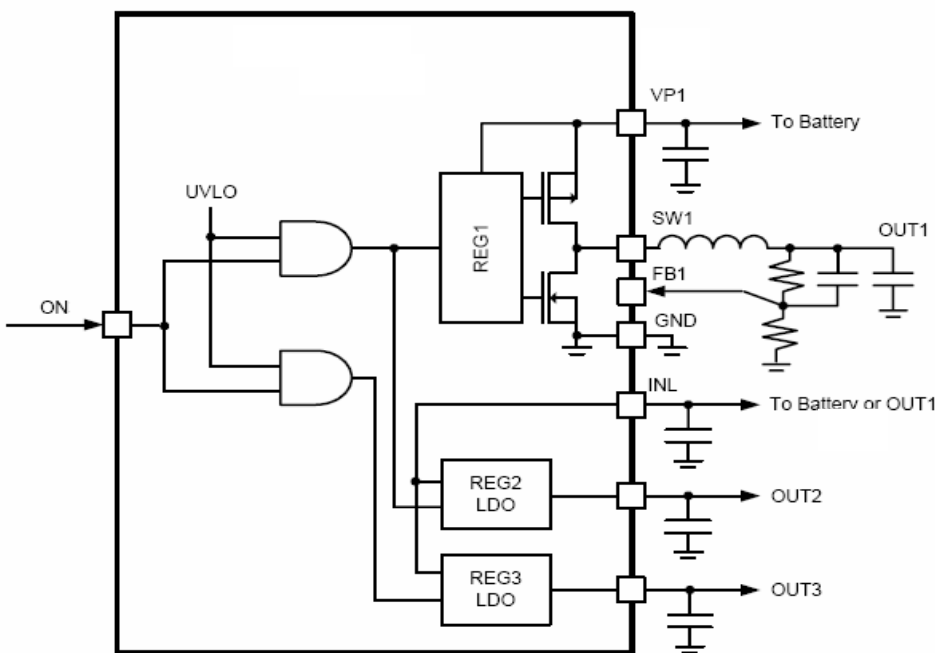


Figure 1. LP78083 High Efficiency Step-Down Converter

Functional Pin Description

Pin Number	Pin Name	Pin Function
1	SW	Ground.
2	GND	Pin For Switching
3	OUT2	Output2,LDO output
4	VIN	Power Input.
5	OUT3	Output3,LDO output
6	EN	DC/DC Chip Enable(Active High).
7	VDD	Power Input.
10	FB	Feedback Input Pin, Reference voltage is 0.6 V

Function Block Diagram



Absolute Maximum Ratings

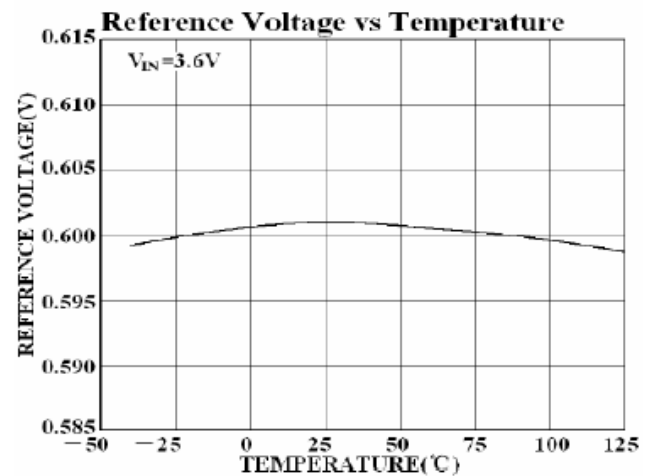
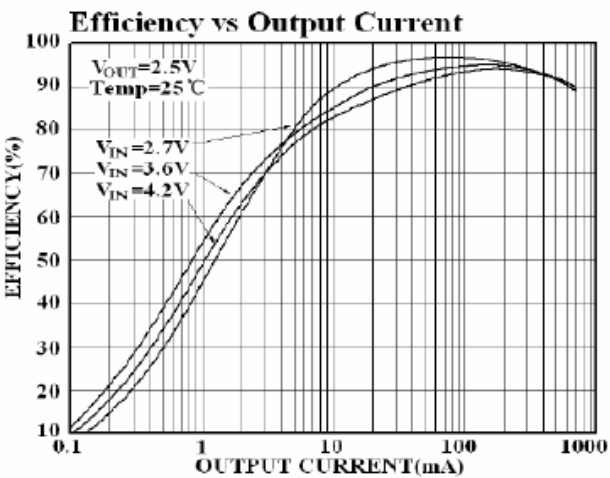
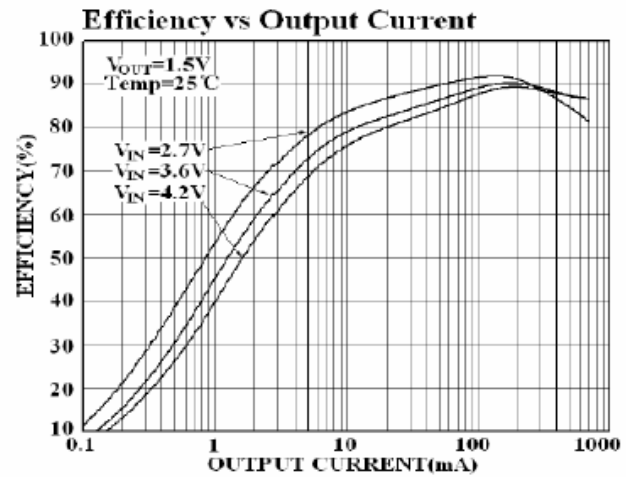
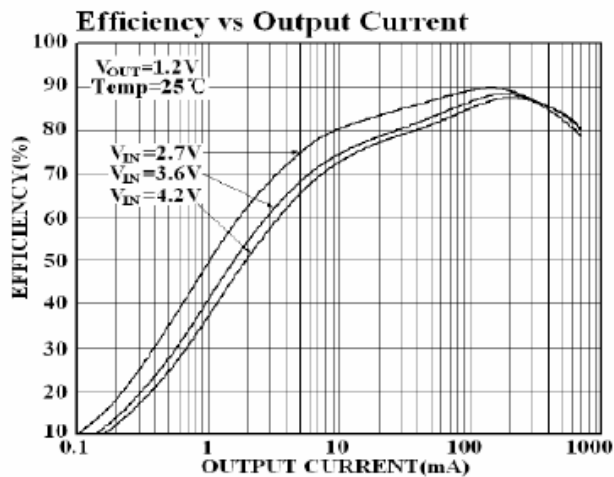
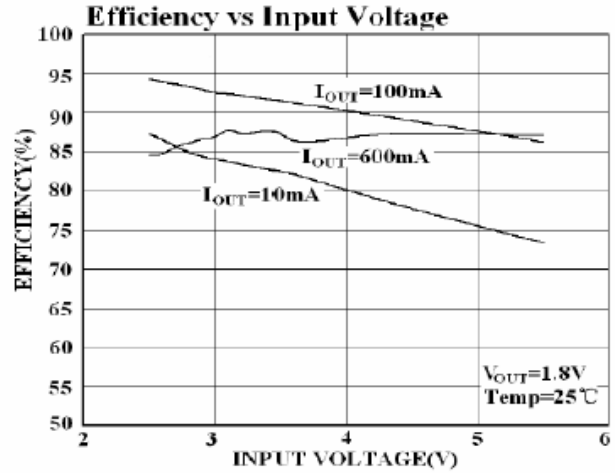
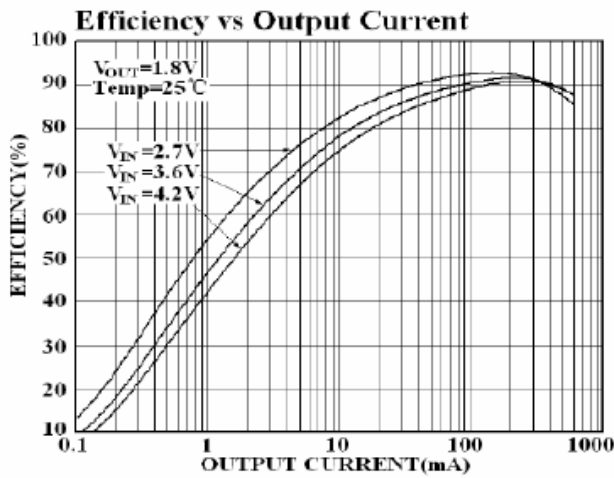
- Input Supply Voltage _____ -0.3V to 6V
- LDO Current _____ 350mA
- P-Channel Switch Source Current(DC) _____ 800mA
- N-Channel Switch Current(DC) _____ 800mA
- Peak SW Sink and Source Current _____ 1100mA
- Operation Temperature Range _____ -40°C to 85°C
- Junction Temperature _____ 125°C
- Storage Temperature _____ -65°C to 150°C
- Lead Temp(Soldering,10sec) _____ 260°C
- ESD Rating(HBM) _____ 2KV

Electrical Characteristics

(VIN = 3.6V, VOUT = 2.5V, VREF = 0.6V, L = 2.2μH, CIN= 4.7μF, COUT= 10μF, TA= 25°C, IMAX = 600mA unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Input Voltage Range	VIN		2.5		5.5	V	
Quiescent Current	IQ	IOUT = 0mA, VFB =0.5V IOUT = 0mA, VFB =0.7V		270 25	350 35	μA	
Shutdown Current	ISHDN	EN = GND		0.1	1	μA	
Reference Voltage	VREF	For adjustable output voltage	0.602	0.612	0.622	V	
Adjustable Output Range	VOUT		VREF		VIN - 0.2	V	
Output Voltage Accuracy	Fixed	Δ VOUT	VIN = 2.2 to 5.5V, VOUT = 1.2V 0A < IOUT < 650mA	-3		+3	%
		Δ VOUT	VIN = 2.2 to 5.5V, VOUT = 1.5V 0A < IOUT < 650mA	-3		+3	%
		Δ VOUT	VIN = 2.2 to 5.5V, VOUT = 1.8V 0A < IOUT < 650mA	-3		+3	%
		Δ VOUT	VIN = 2.8 to 5.5V, VOUT = 2.5V 0A < IOUT < 650mA	-3		+3	%
		Δ VOUT	VIN = 3.5 to 5.5V, VOUT = 3.3V 0A < IOUT < 650mA	-3		+3	%
	Adjustable	Δ VOUT	VIN = VOUT + 0.2V to 5.5V, VIN ≧ 3.5V 0A < IOUT < 650mA	-3		+3	%
		Δ VOUT	VIN = VOUT + 0.4V to 5.5V, VIN ≧ 2.2V 0A < IOUT < 650mA	-3		+3	%
LDO Output current	ILDO		300	350	400	mA	
PMOSFET RON	PRDS(ON)	IOUT = 200mA VIN = 3.6V		0.45	0.53	Ω	
NMOSFET RON	NRDS(ON)	IOUT = 200mA VIN = 3.6V		0.45		Ω	
P-Channel Current Limit	IP(LM)	VIN =2.2 to 5.5V	600	800	1000	mA	
EN Threshold	VEN		0.8	1.2	1.5	V	
EN Leakage Current	VENL		--	2		μA	

Typical Operating Characteristics



Applications Information

The basic LP78083 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor selection

The output inductor is selected to limit the ripple current to some predetermined value. typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is $\Delta I_L = 180\text{mA}$ (40% of 650mA).

$$\Delta I_L = \frac{1}{f(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated Inductor should be enough for most applications (650mA+120mA). For better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor Sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN}=2V_{OUT}, where I_{RMS}=I_{OUT}/2. this simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the Capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective

series resistance(ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in later section. the output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

Using ceramic input and output capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes, their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. however care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output voltage programming

The output voltage is set by a resistive divider according to the

Following formula:

$$V_{OUT} = 0.6V \left(1 + \frac{R2}{R1} \right)$$

The external resistive divider is connected to the output, allowing Remote voltage sensing as shown in figure3.

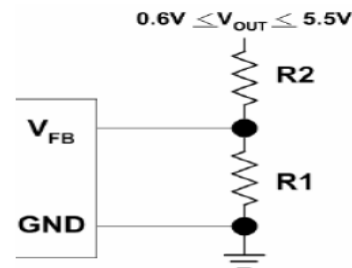


Figure3.

Efficiency considerations

The efficiency of a switching regulator is equal to the output Power divided by the input power times 100%.it is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement efficiency can be expressed as :

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 \dots)$$

Where L1、 L2, etc. are the individual losses as a percentage of Input power .although all dissipative elements in the for most of losses: VIN quiescent current and I²R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1.The VIN quiescent current is due to two components: the DC Bias current as given in the electrical characteristics and the Internal main switch and synchronous switch gate charge currents. the gate charge current results from switching the gate capacitance of the internal power MOSFET switches .Each time the gate charge current.results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switches from high to low to high again, a packet of charge ΔQ moves from VIN to ground.

The resulting ΔQ/Δt is the current out of VIN that is typically larger than the DC bias current. In continuous mode.

$$I_{GATCHG} = f(Q_T + Q_B)$$

Where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I²R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor RL. in continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET R_{DS(ON)} and the duty cycle (DC) as follows:

$$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1 - DC)$$

The R_{DS(ON)} for both the top and bottom MOSFETS can be obtained from the typical performance characteristics curves. thus, to obtain I²R losses, simply add R_{SW} to RL and multiply the square of the average output current.

Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Checking Transient Response

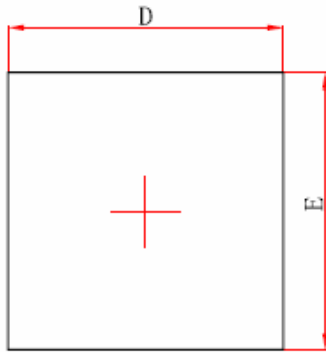
The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of COUT. ΔI_{LOAD} also begins to charge or discharge COUT generating a feedback error signal used by the regulator to return VOUT to its steady-state value. During this recovery time, VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

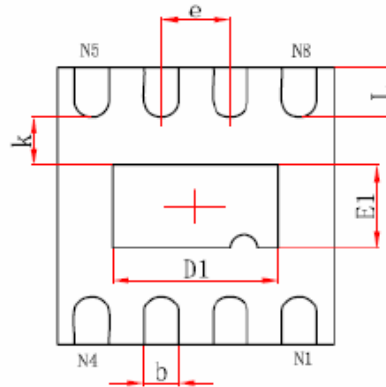
- ✧ Follow the PCB layout guidelines for optimal performance of LP78083.
- ✧ For the main current paths as indicated in bold lines, keep their traces short and wide.
- ✧ Put the input capacitor as close as possible to the device pins (VIN and GND).
- ✧ LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- ✧ Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the LP78083.
- ✧ Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information

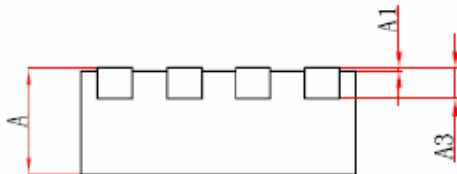
DFN2*2-8L Package Outline Dimension



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.006	0.010
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E1	0.500	0.700	0.020	0.028
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.250	0.450	0.010	0.018