

## 250mA, Dual Channel Ultra-Fast CMOS LDO Regulator

### General Description

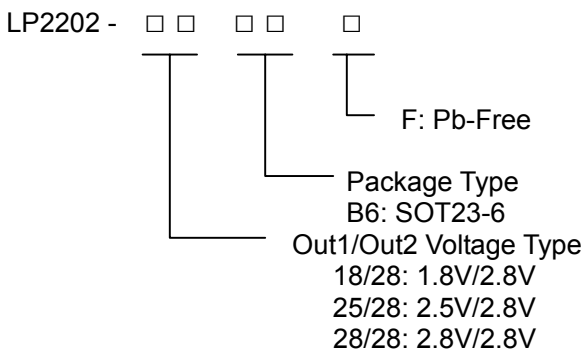
The LP2202 is a dual channel, low noise, and low dropout regulator sourcing up to 250mA at each channel. The range of output voltage is from 1.2V to 3.6V by operating from 2.5V to 5.5V input.

LP2202 offers 2% accuracy, extremely low dropout voltage (220mV @ 250mA), and extremely low ground current, only 25µA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection.

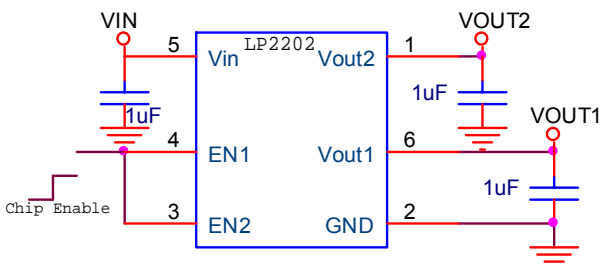
LP2202 is short circuit thermal folded back protected. LP2202 lowers its OTP trip point from 165°C to 110°C when output short circuit occurs ( $V_{OUT} < 0.4V$ ) providing maximum safety to end users.

LP2202 can operate stably with very small ceramic output capacitors, reducing required board space and component cost. LP2202 is available in fixed output voltages in the SOT-23-6 package.

### Ordering Information



### Typical Application Circuit



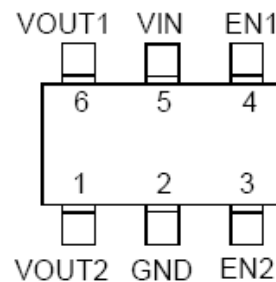
### Features

- ◆ Wide Operating Voltage Ranges : 2.5V to 5.5V
- ◆ Low-Noise for RF Application
- ◆ High PSRR 70dB at 1kHz
- ◆ No Noise Bypass Capacitor Required
- ◆ Fast Response in Line/Load Transient
- ◆ TTL-Logic-Controlled Shutdown Input
- ◆ Dual LDO Outputs (300mA/300mA)
- ◆ High Output Accuracy 2%
- ◆ Ultra-low Quiescent Current 27uA
- ◆ Thermal Shutdown Protection
- ◆ Thermal Shutdown Protection
- ◆ Tiny SOT-23-6 and 8-Lead DFN Package
- ◆ RoHS Compliant and 100% Lead (Pb)-Free

### Applications

- ✧ CDMA/GSM Cellular Handsets
- ✧ Smart mobile phone
- ✧ Battery-Powered Equipment
- ✧ DSC Sensor
- ✧ Wireless Card

### Pin Configurations



SOT23-6 (Top View)

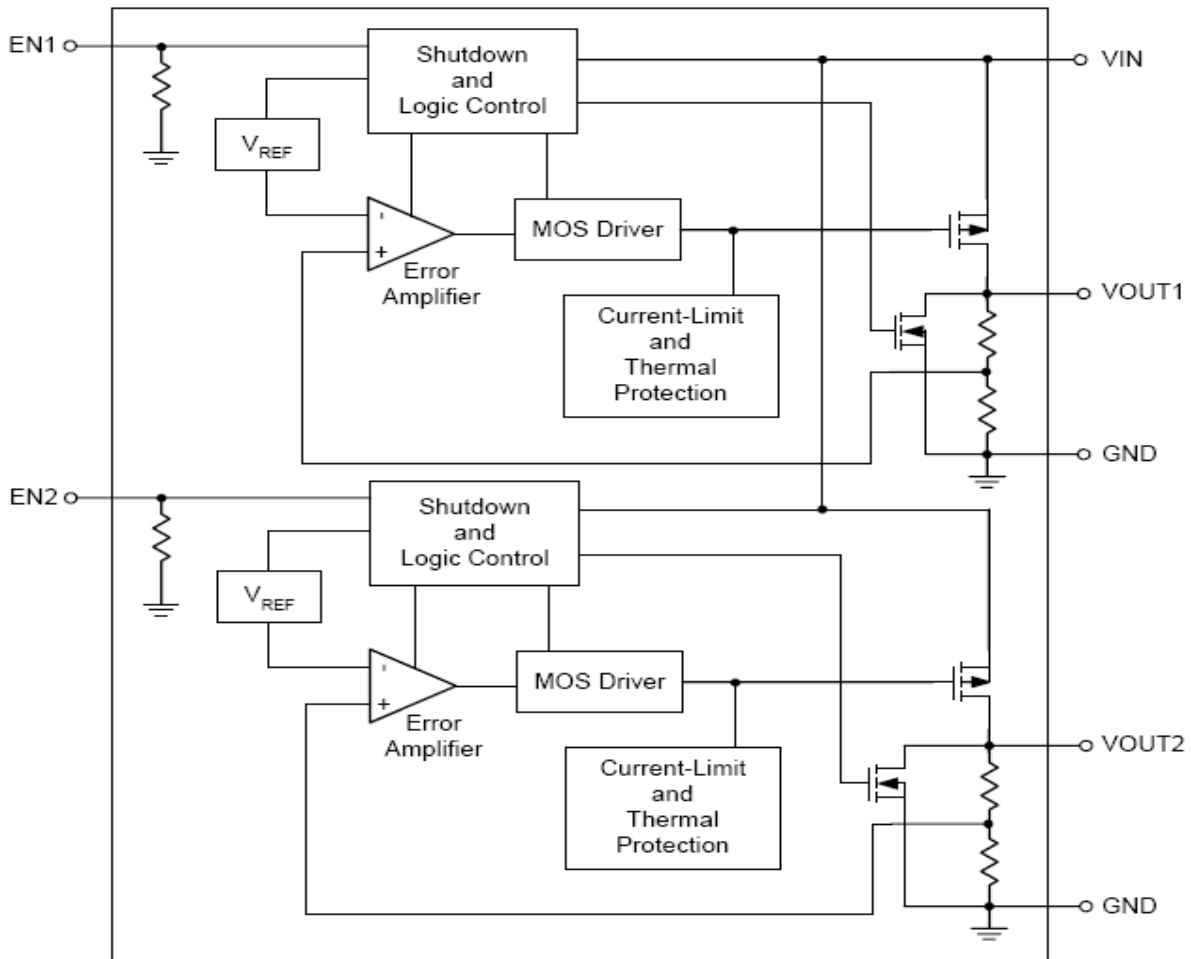
### Marking Information

Please see website.

### Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT2	Channel 2 Output Voltage
2	GND	Common Ground
3	EN2	Chip Enable2 (Active High)
4	EN1	Chip Enable1 (Active High)
5	VIN	Supply Input
6	VOUT1	Channel 1 Output Voltage

### Function Block Diagram



### Absolute Maximum Ratings

Supply Input Voltage	-----6V
Power Dissipation, PD @ TA = 25° C	
SOT23-6	-----455mW
Package Thermal Resistance	
SOT23-6, $\theta_{JA}$	-----220°C/W
Lead Temperature (Soldering, 10 sec.)	-----260°C
Storage Temperature Range	----- -65°C to 150°C
ESD Susceptibility	
HBM (Human Body Mode)	-----2kV
MM(Machine-Mode)	-----200V
Recommended Operating Conditions	
Operation Junction Temperature Range	----- -40°C to 125°C
Operation Ambient Temperature Range	----- -40°C to 85°C

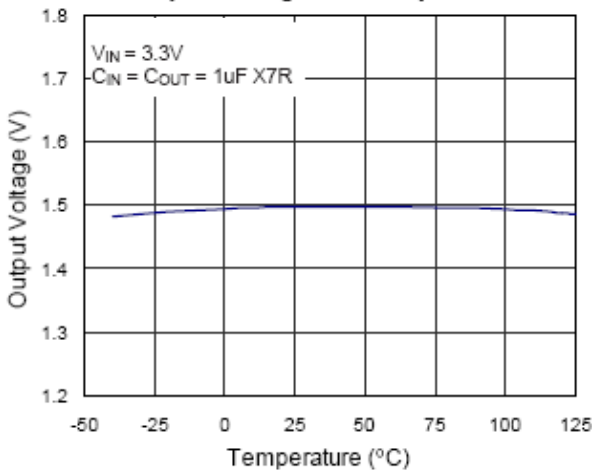
### Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1 $\mu$ F, TA = 25° C, unless otherwise specified)

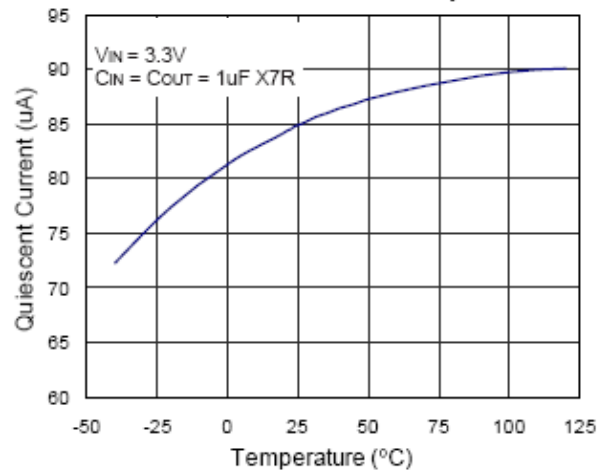
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy	$\Delta V_{OUT}$	IOUT = 1mA	-2	--	+2	%
Current Limit	ILIM	RLOAD = 1 $\Omega$	360	450	700	mA
Quiescent Current	IQ	VEN $\geq$ 1.2V, IOUT = 0mA		75	110	$\mu$ A
Dropout Voltage	VDROP	IOUT = 200mA, VOUT > 2.8V		170	200	mV
		IOUT = 250mA, VOUT > 2.8V		220	300	
Line Regulation	$\Delta V_{LINE}$	VIN = (VOUT + 1V) to 5.5V, IOUT = 1mA			0.3	%
Load Regulation	$\Delta V_{LOAD}$	1mA < IOUT < 300mA			0.6	%
Standby Current	ISTBY	VEN = GND, Shutdown		0.01	1	$\mu$ A
EN Input Bias Current	IIBSD	VEN = GND or VIN		0	100	nA
EN Threshold	Logic-Low Voltage	VIL			0.4	V
	Logic-High Voltage	VIH	1.2			
Output Noise Voltage		10Hz to 100kHz, IOUT = 200mA COUT = 1 $\mu$ F		100		$\mu$ VRMS
Power Supply Rejection Rate	f = 100Hz f = 10kHz	PSRR		-75 -65		dB
Thermal Shutdown Temperature	TSD			165		°C

## Typical Operating Characteristics

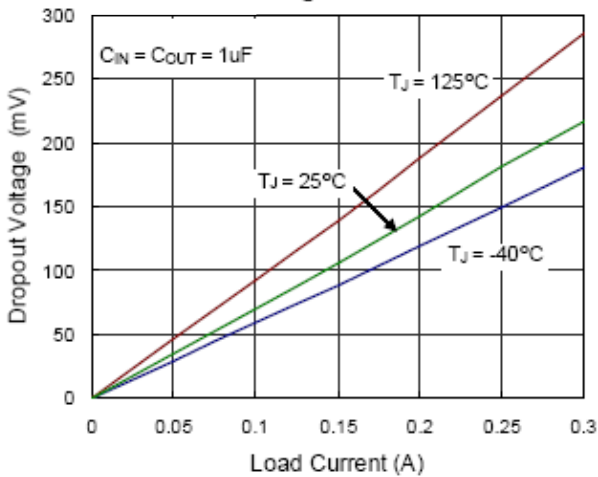
Output Voltage vs. Temperature



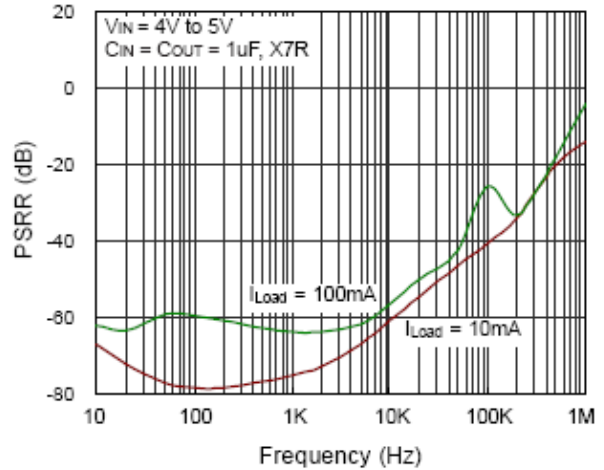
Quiescent Current vs. Temperature



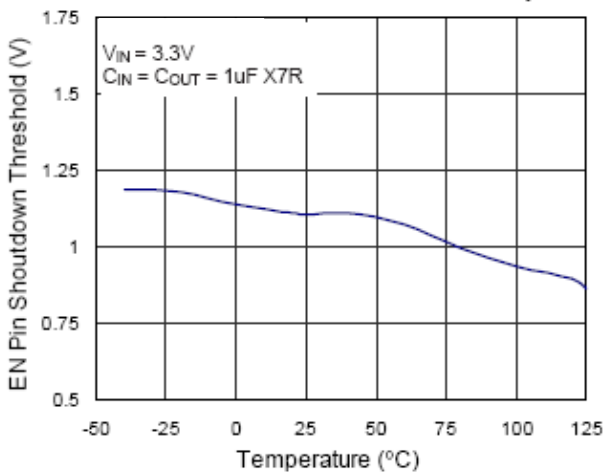
Dropout Voltage vs. Load Current



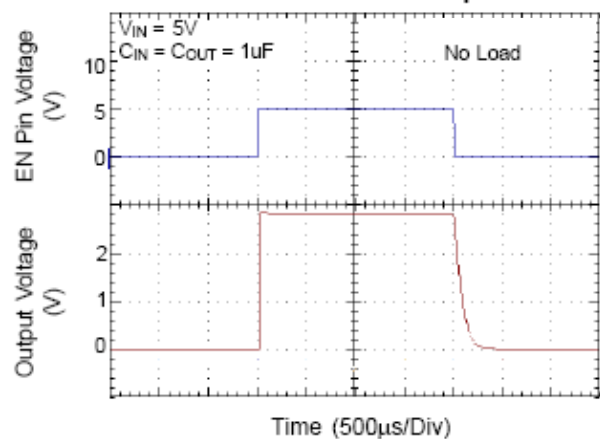
PSRR



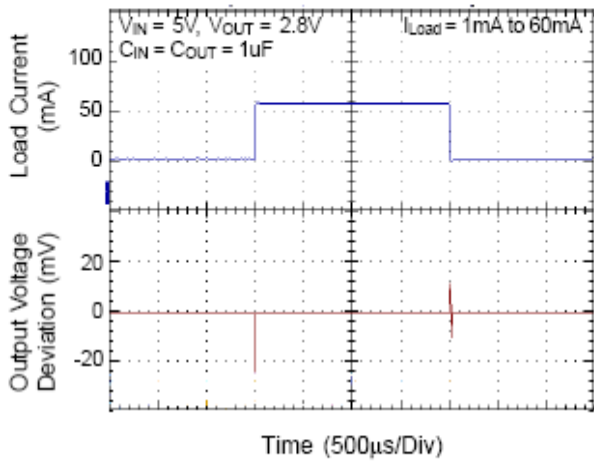
EN Pin Shutdown Threshold vs. Temperature



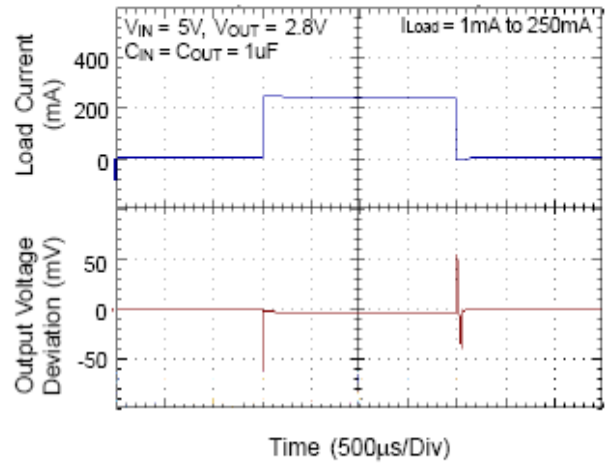
EN Pin Shutdown Response



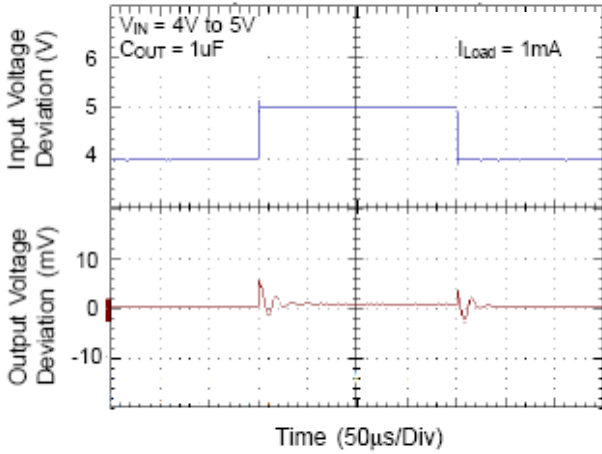
Load Transient Response



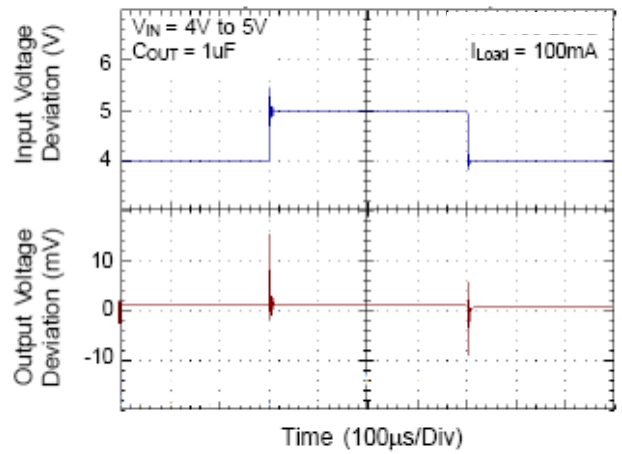
Load Transient Response



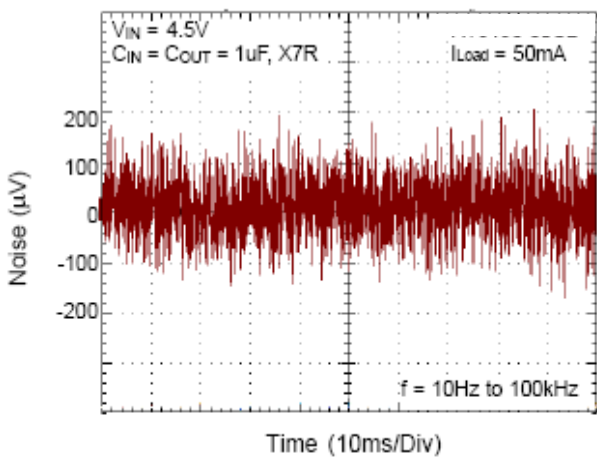
Line Transient Response



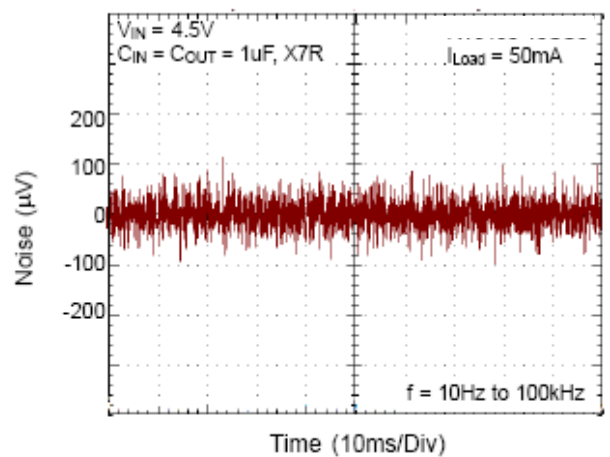
Line Transient Response



Noise



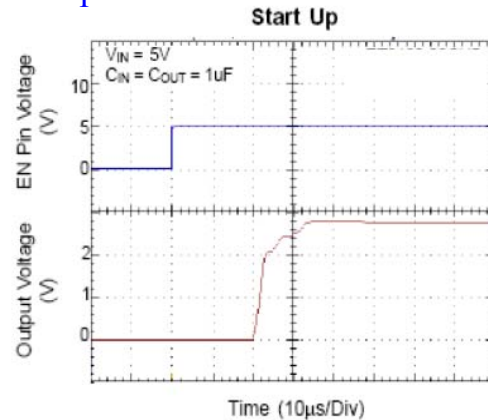
Noise



## Applications Information

Like any low-dropout regulator, the external capacitors used with the LP2202 must be carefully selected for regulator stability and performance. Using a capacitor whose value is  $> 1\mu\text{F}$  on the LP2202 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP2202 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least  $1\mu\text{F}$  with ESR is  $> 25\text{m}\Omega$  on the LP2202 output ensures stability. The LP2202 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP2202 and returned to a clean analog ground.

## Start-up Function Enable Function



The LP2202 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For protecting the system, the LP2202 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

## Thermal Considerations

Thermal protection limits power dissipation in LP2202. When the operation junction temperature exceeds  $165^{\circ}\text{C}$ , the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by  $30^{\circ}\text{C}$ . For continue operation, do not exceed absolute maximum operation junction temperature  $125^{\circ}\text{C}$ .

The power dissipation definition in device is :

$$PD = (VIN - VOUT) \times IO_{OUT} + VIN \times IQ$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula :

$$PD(\text{MAX}) = (TJ(\text{MAX}) - TA) / \theta_{JA}$$

Where TJ(MAX) is the maximum operation junction

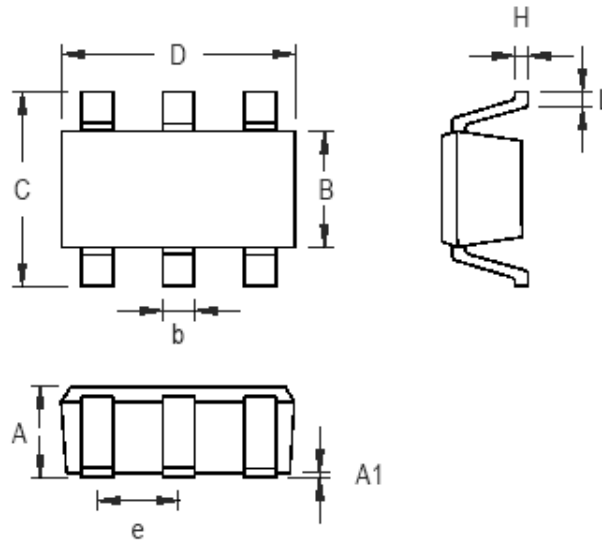
temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of LP2202, where  $T_{J(MAX)}$  is the maximum junction temperature of the die (125°C) and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance ( $\theta_{JA}$  is layout dependent) for SOT23-6 package is 250°C/W.

$$PD(MAX) = (125^{\circ}C - 25^{\circ}C) / 250 = 400mW \text{ (SOT23-6)}$$

$$PD(MAX) = (125^{\circ}C - 25^{\circ}C) / 165 = 606mW$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ .

Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

**SOT-23-6 Surface Mount Package**