

**1.5MHz, 650mA, High Efficiency Synchronous**

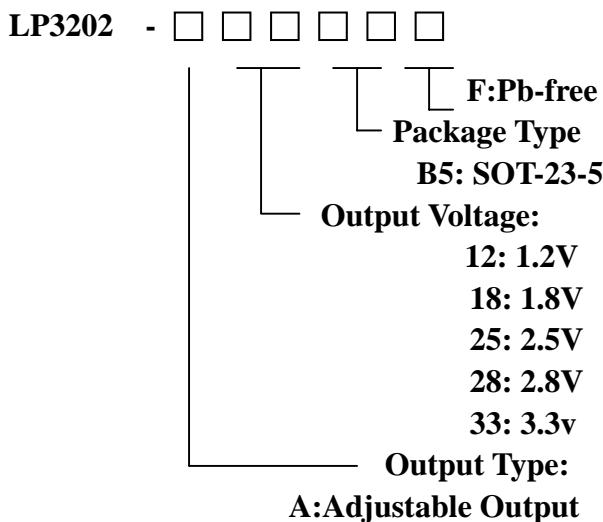
**PWM Step-Down DC/DC Convert**

**General Description**

The LP3202 is a constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency. The 2.1V to 5.5V input voltage range makes the LP3202 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy-terminals.

Internal synchronous rectifier with low RDS(ON) dramatically reduces conduction loss at PWM mode. The internal synchronous switch increases efficiency while eliminate the need for an external Schottky diode. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small SOT-23-5 package provide small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

**Ordering Information**



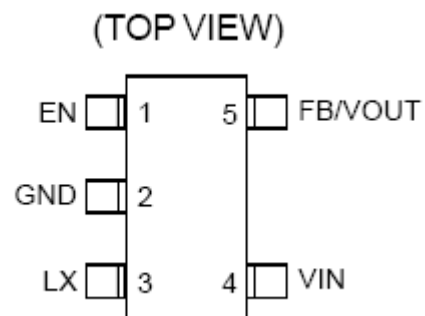
**Features**

- ◆ High Efficiency: 93%
- ◆ 1.5MHz Fixed-Frequency PWM Operation
- ◆ Adjustable Output From 0.6V to VIN
- ◆ 1.2V, 1.5V, 1.8V, 2.5V, 2.8V and 3.3V Fixed
- ◆ 650mA Output Current, 1.1A Peak Current
- ◆ No Schottky Diode Required
- ◆ 100% Duty Cycle Low Dropout Operation
- ◆ Available in SOT23-5 Package
- ◆ Short Circuit and Thermal Protection
- ◆ Over Voltage Protection
- ◆ Low than 1µA Shutdown Current

**Applications**

- ◇ Portable Media Players/MP3 players
- ◇ Cellular and Smart mobile phone
- ◇ PDA
- ◇ DSC
- ◇ Wireless Card

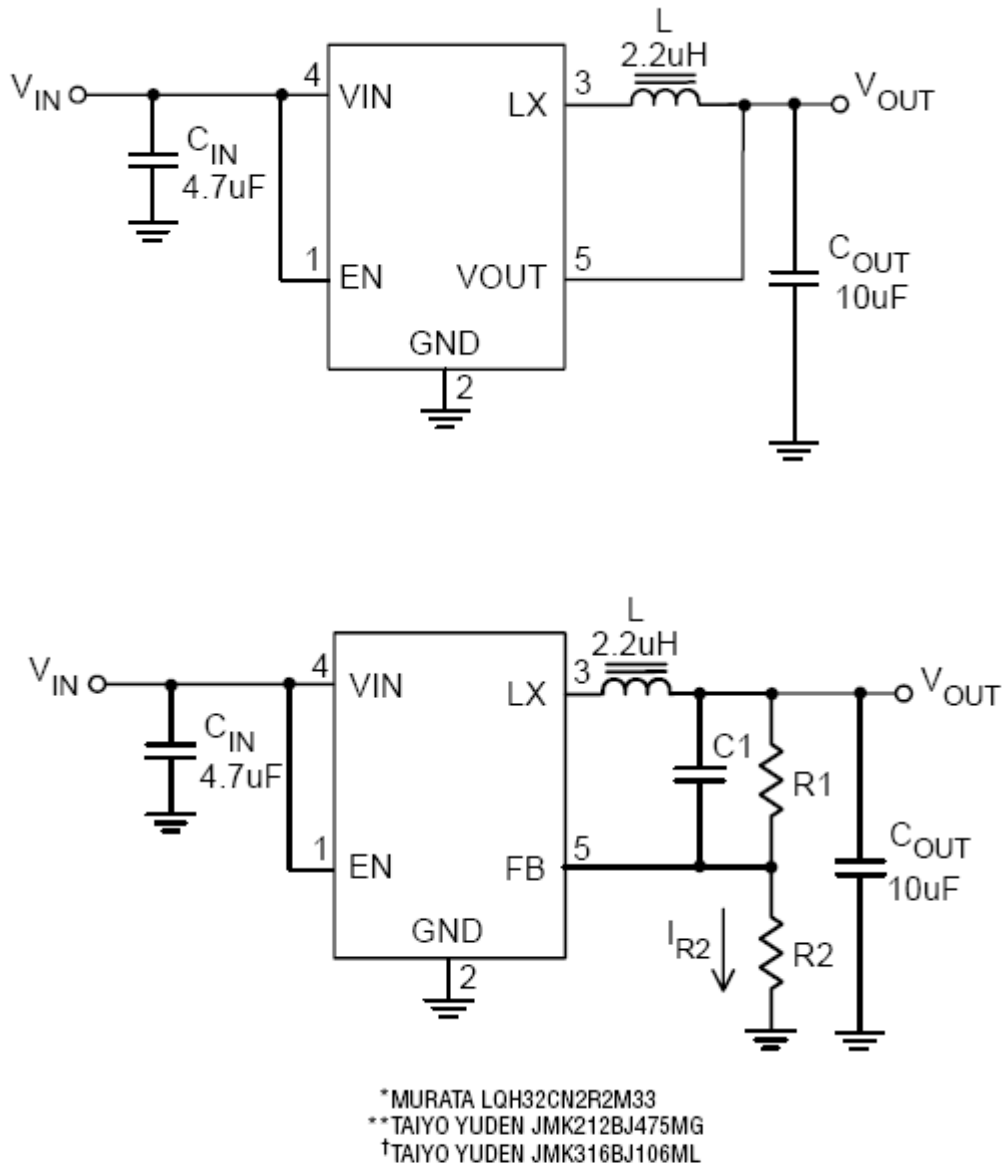
**Pin Configurations**



**Marking Information**

Please See website.

**Typical Application Circuit**

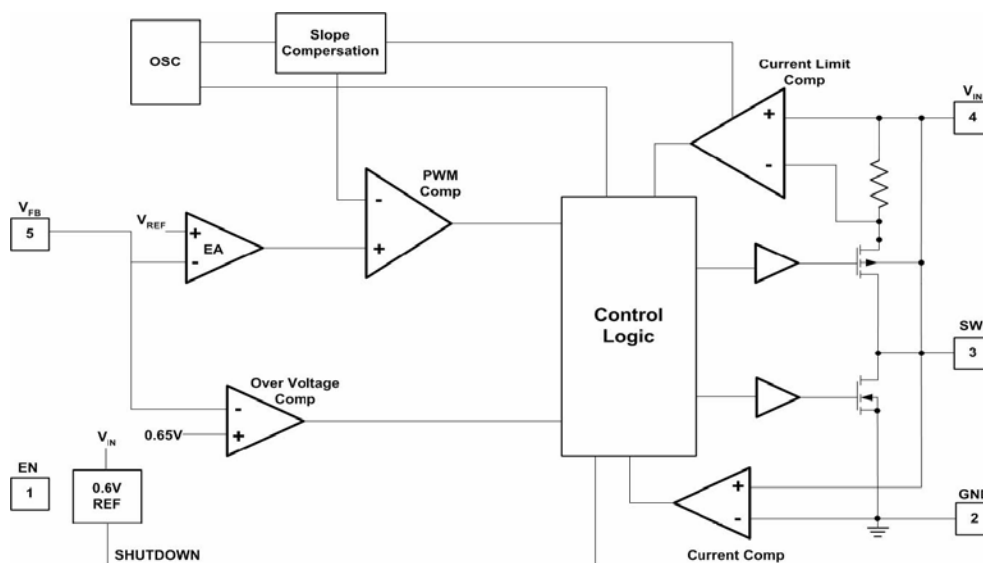


**Figure 1a. High Efficiency Step-Down Converter**

## Functional Pin Description

| Pin Number | Pin Name | Pin Function               |
|------------|----------|----------------------------|
| 1          | EN       | Chip Enable (Active High). |
| 2          | GND      | Ground.                    |
| 3          | LX       | Pin for Switching.         |
| 4          | VIN      | Power Input.               |
| 5          | FB/VOUT  | Feedback Input Pin.        |

## Function Block Diagram



## Absolute Maximum Ratings

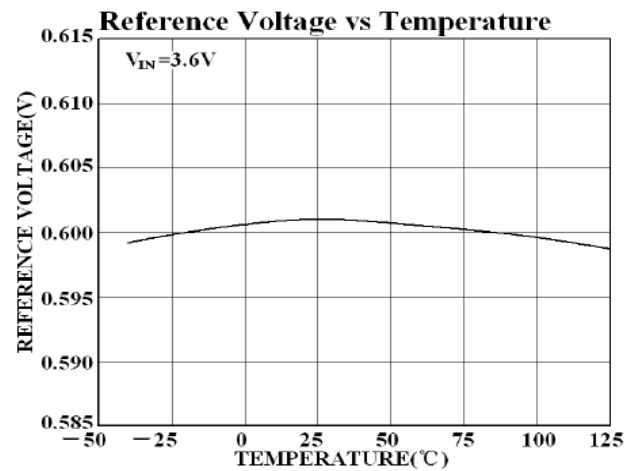
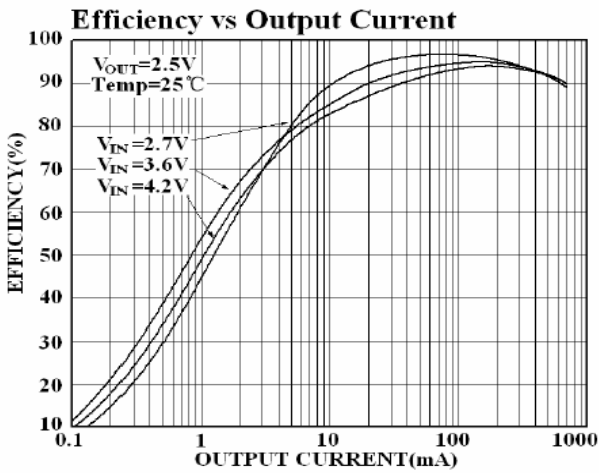
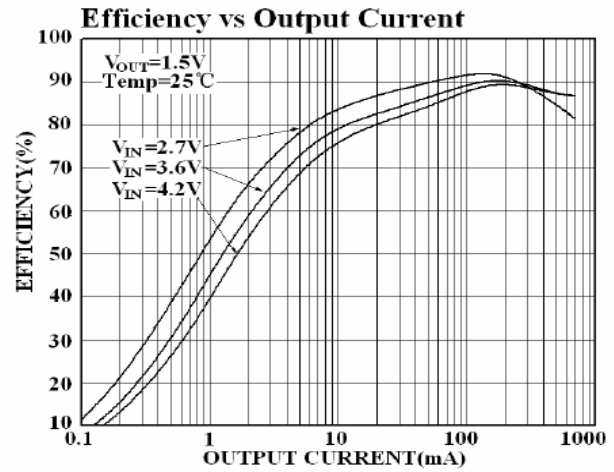
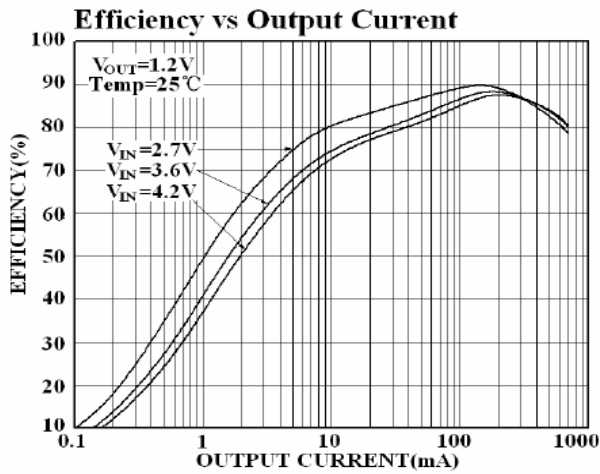
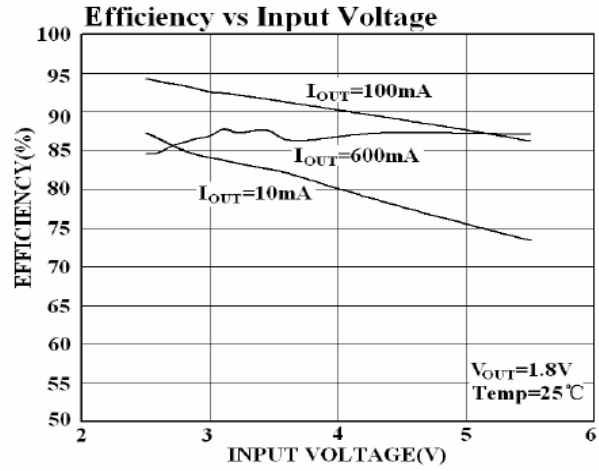
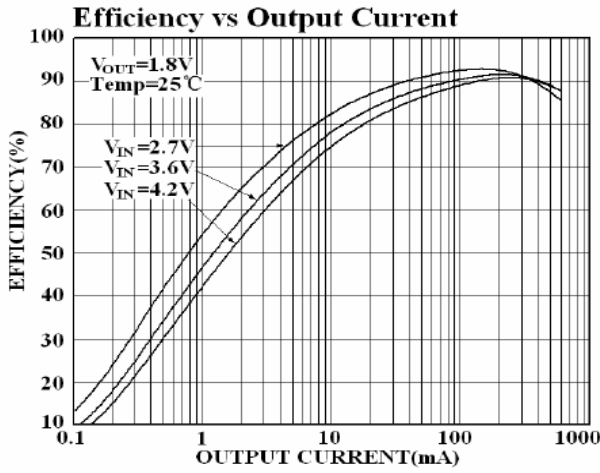
- Input Supply Voltage ----- -0.3V to 6V
- EN, VFB Voltages ----- -0.3V to  $V_{IN}$
- P-Channel Switch Source Current (DC) ----- 800mA
- N-Channel Switch Sink Current (DC) ----- 800mA
- Peak SW Sink and Source Current ----- 1.4A
- Operating Temperature Range ----- -40°C to 85°C
- Junction Temperature ----- 125°C
- Storage Temperature ----- -65°C to 150°C
- Lead Temp (Soldering, 10sec) ----- 260°C
- ESD Rating (HBM) ----- 2kV

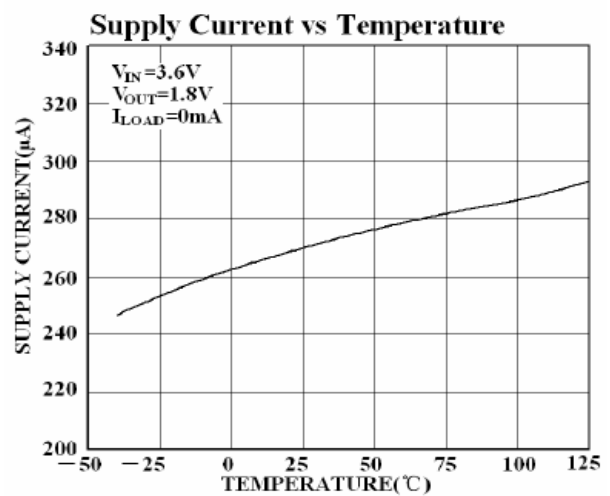
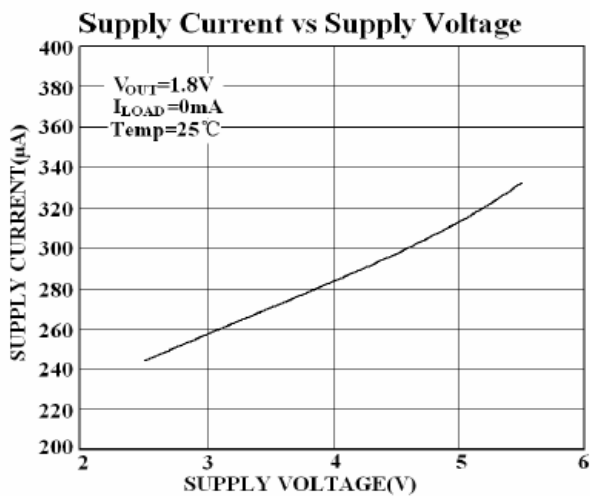
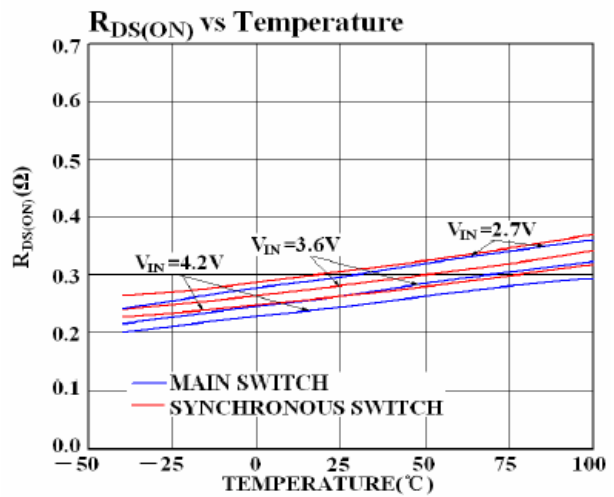
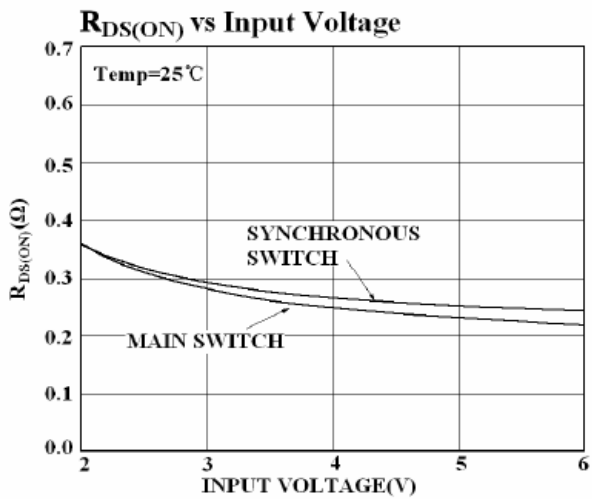
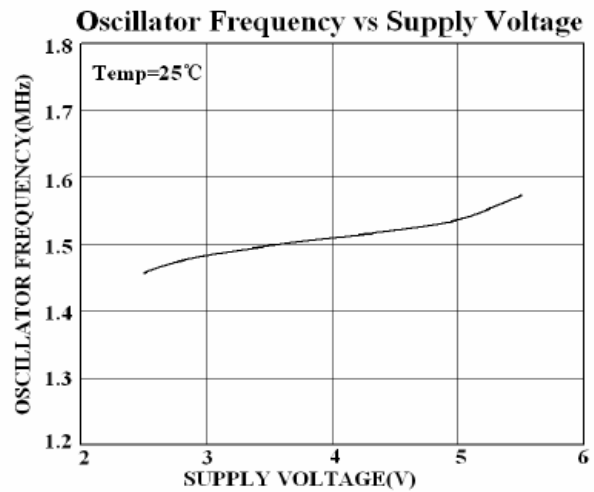
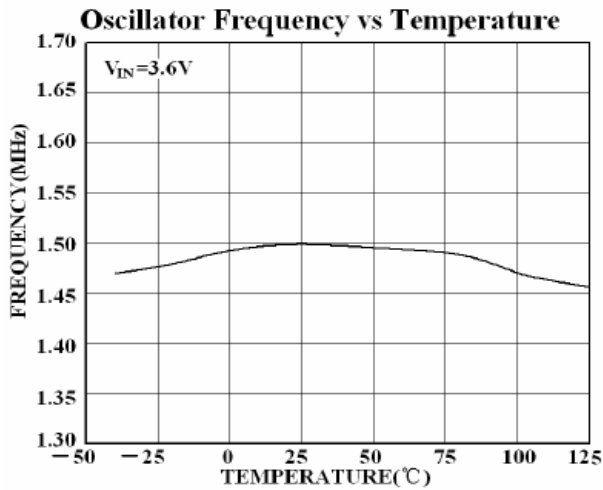
## Electrical Characteristics

(VIN = 3.6V, VOUT = 2.5V, VREF = 0.6V, L = 2.2μH, CIN= 4.7μF, COUT= 10μF, TA= 25°C, IMAX = 650mA unless otherwise specified)

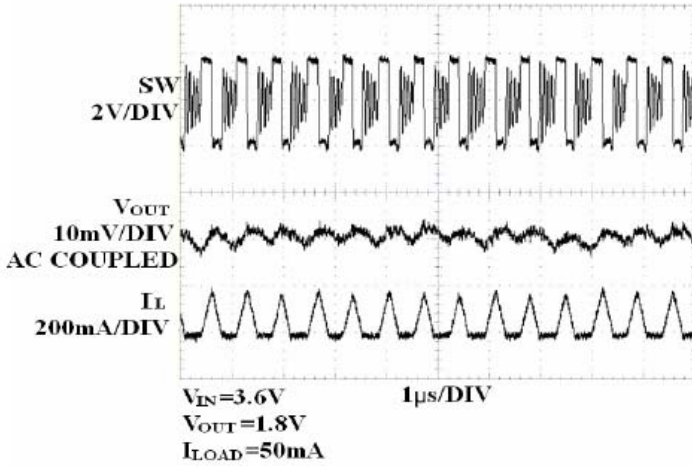
| Parameter               | Symbol               | Test Conditions                                         | Min   | Typ  | Max       | Units |
|-------------------------|----------------------|---------------------------------------------------------|-------|------|-----------|-------|
| Input Voltage Range     | VIN                  |                                                         | 2.5   |      | 5.5       | V     |
| Quiescent Current       | IQ                   | IOUT = 0mA, VFB = VREF + 5%                             |       | 270  | 370       | μA    |
| Shutdown Current        | ISHDN                | EN = GND                                                |       | 0.1  | 1         | μA    |
| Reference Voltage       | VREF                 | For adjustable output voltage                           | 0.588 | 0.6  | 0.612     | V     |
| Adjustable Output Range | VOUT                 |                                                         | VREF  |      | VIN - 0.2 | V     |
|                         | Δ VOUT               | VIN = 2.2 to 5.5V, VOUT = 1.0V 0A < IOUT < 600mA        | -3    |      | +3        | %     |
|                         | Δ VOUT               | VIN = 2.2 to 5.5V, VOUT = 1.2V 0A < IOUT < 600mA        | -3    |      | +3        | %     |
|                         | Fix<br>Δ VOUT        | VIN = 2.2 to 5.5V, VOUT = 1.5V 0A < IOUT < 600mA        | -3    |      | +3        | %     |
| Output Voltage Accuracy | Δ VOUT               | VIN = 2.2 to 5.5V, VOUT = 1.8V 0A < IOUT < 600mA        | -3    |      | +3        | %     |
|                         |                      | VIN = 2.8 to 5.5V, VOUT = 2.5V 0A < IOUT < 600mA        | -3    |      | +3        | %     |
|                         |                      | VIN = 3.5 to 5.5V, VOUT = 3.3V 0A < IOUT < 600mA        | -3    |      | +3        | %     |
|                         | Adjustable<br>Δ VOUT | VIN = VOUT + 0.2V to 5.5V, VIN ≧ 3.5V 0A < IOUT < 600mA | -3    |      | +3        | %     |
|                         |                      | VIN = VOUT + 0.4V to 5.5V, VIN ≧ 2.2V 0A < IOUT < 600mA | -3    |      | +3        | %     |
| FB Input Current        | IFB                  | VFB = VIN                                               | -30   |      | 30        | nA    |
| PMOSFET RON             | PRDS(ON)             | IOUT = 200mA<br>VIN = 3.6V                              |       | 0.20 | 0.38      | Ω     |
| NMOSFET RON             | NRDS(ON)             | IOUT = 200mA<br>VIN = 3.6V                              |       | 0.25 |           | Ω     |
| P-Channel Current Limit | IP(LM)               | VIN = 2.2 to 5.5 V                                      | 1     | 1.2  | 1.4       |       |
| EN Threshold            | VEN                  |                                                         | 0.3   | 1.0  | 1.5       | V     |
| EN Leakage Current      | VENL                 |                                                         | --    | 1    |           | uA    |

## Typical Operating Characteristics

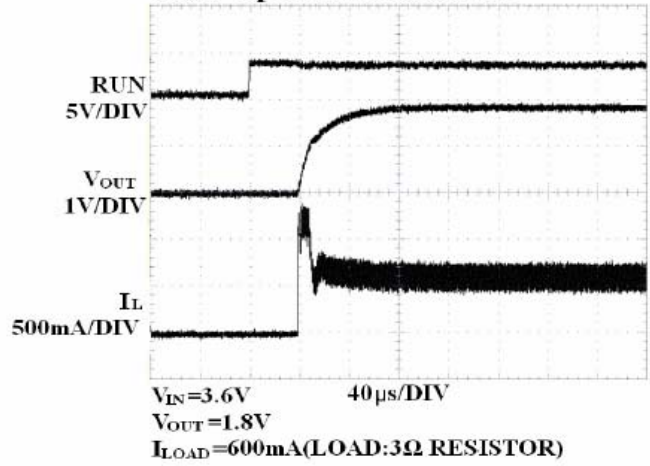




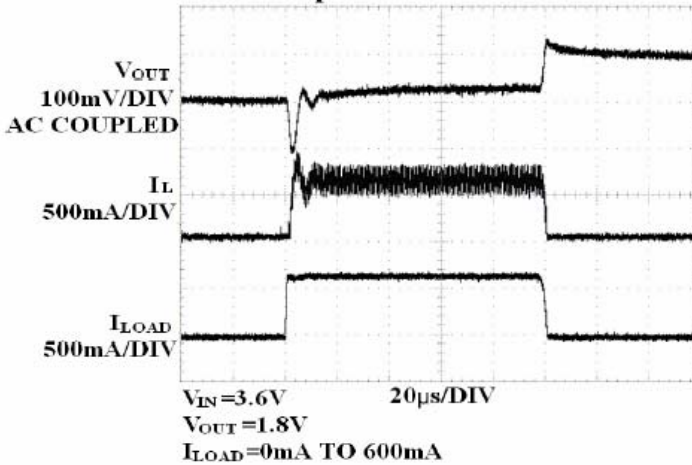
**Discontinuous Operation**



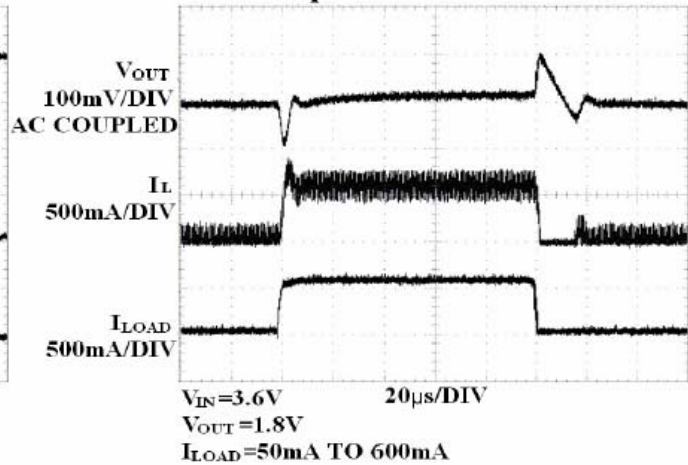
**Start-Up from Shutdown**



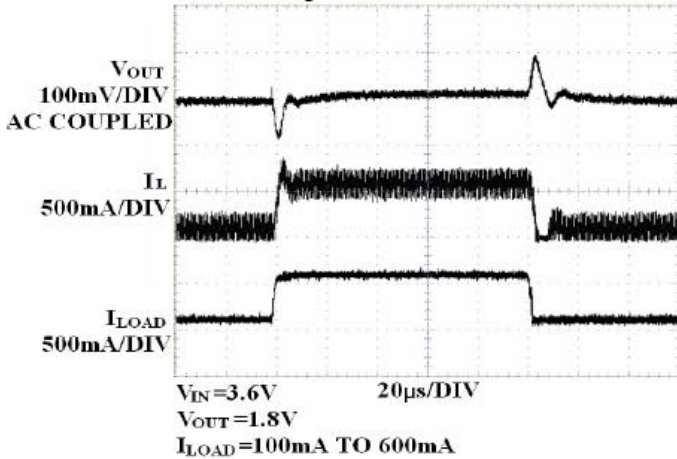
**Load Step**



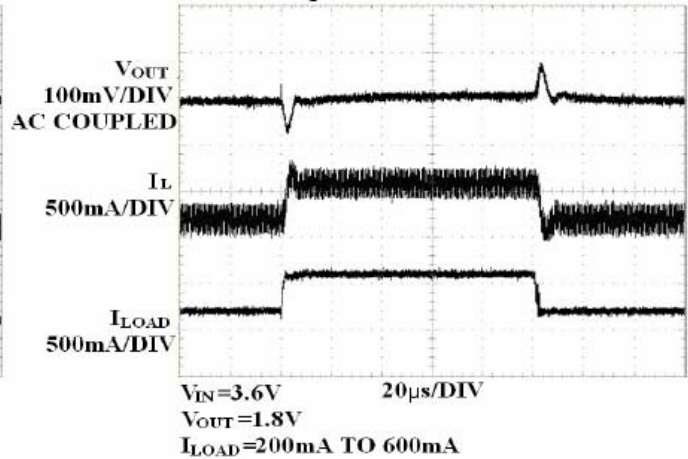
**Load Step**



**Load Step**



**Load Step**



## Applications Information

The basic LP3202 application circuit is shown in **Typical Application Circuit**. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by  $C_{IN}$  and  $C_{OUT}$ .

### Inductor Selection

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is  $\Delta I_L = 240\text{mA}$  (40% of 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be enough for most applications (600mA+120mA). For better efficiency, choose a low DC-resistance inductor.

### $C_{IN}$ and $C_{OUT}$ Selection

The input capacitance,  $C_{IN}$ , is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from

capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of  $C_{OUT}$  is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple,  $\Delta V_{OUT}$ , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ \text{ESR} + \frac{1}{8fC_{OUT}} \right]$$

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input,  $V_{IN}$ . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at  $V_{IN}$  large enough to damage the part.

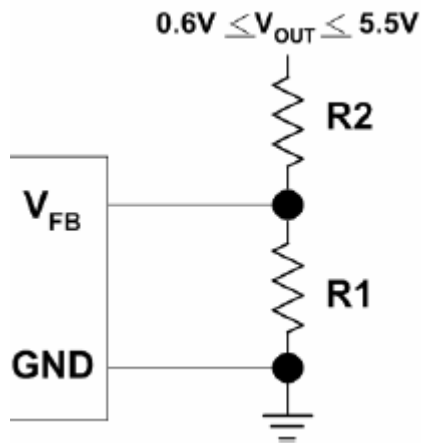
### Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V \left( 1 + \frac{R2}{R1} \right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure3.





**Figure3.**

**Efficiency Considerations**

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses :  $V_{IN}$  quiescent current and  $I^2R$  losses. The  $V_{IN}$  quiescent current loss dominates the efficiency loss at very low load currents whereas the  $I^2R$  loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The  $V_{IN}$  quiescent current is due to two components : the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge  $\Delta Q$  moves from  $V_{IN}$  to ground.

The resulting  $\Delta Q/\Delta t$  is the current out of  $V_{IN}$  that is typically larger than the DC bias current. In continuous mode,

$$I_{GATECHG} = f(Q_T + Q_B)$$

where  $Q_T$  and  $Q_B$  are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to  $V_{IN}$  and thus their effects will be more pronounced at higher supply voltages.

2.  $I^2R$  losses are calculated from the resistances of the internal switches,  $R_{SW}$  and external inductor  $R_L$ . In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET  $R_{DS(ON)}$  and the duty cycle (DC) as follows :

$$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$$

The  $R_{DS(ON)}$  for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain  $I^2R$  losses, simply add  $R_{SW}$  to  $R_L$  and multiply the result by the square of the average output current.

Other losses including  $C_{IN}$  and  $C_{OUT}$  ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

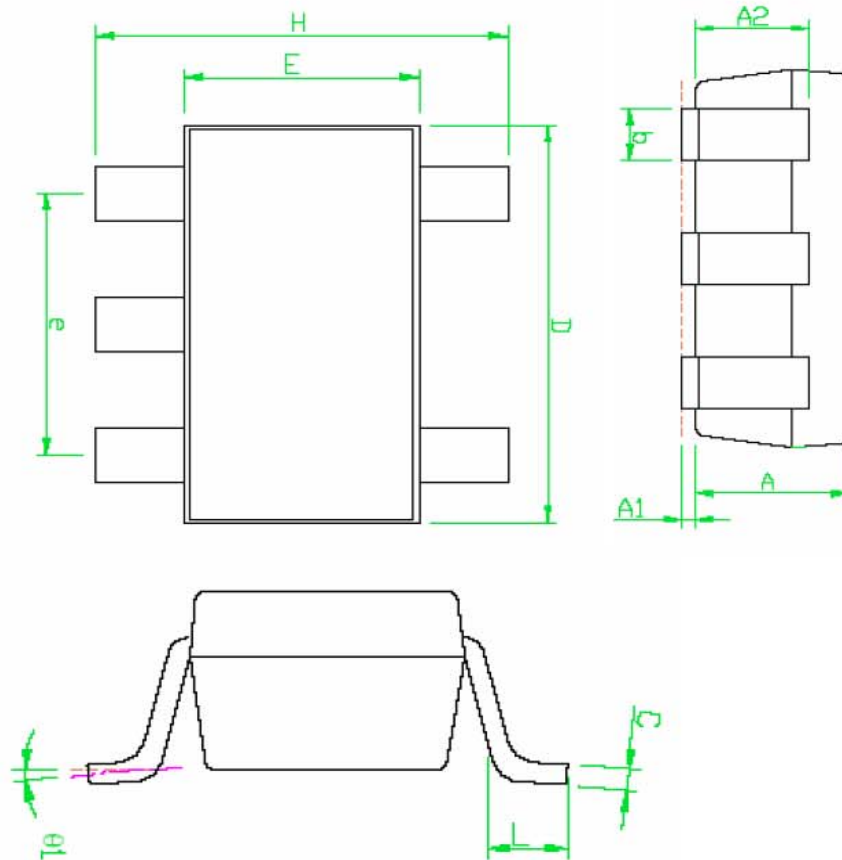
## Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to  $\Delta I_{LOAD}$  (ESR), where ESR is the effective series resistance of COUT.  $\Delta I_{LOAD}$  also begins to charge or discharge COUT generating a feedback error signal used by the regulator to return VOUT to its steady-state value. During this recovery time, VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

## Layout Considerations

- Follow the PCB layout guidelines for optimal performance of LP3202.
- For the main current paths as indicated in bold lines, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the LP3202.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information



Note:

1. Package body sizes exclude mold flash protrusions or gate burrs.
2. Tolerance  $\pm 0.1000\text{mm}$  (4 mil) unless otherwise specified.
3. Coplanarity: 0.1000mm
4. Dimension L is measured in gage plane.

| Symbols  | Dimension in Millimeters |            |       |
|----------|--------------------------|------------|-------|
|          | Min.                     | Nom        | Max.  |
| A        | 1.00                     | 1.10       | 1.30  |
| A1       | 0.00                     | -----      | 0.10  |
| A2       | 0.70                     | 0.80       | 0.90  |
| b        | 0.35                     | 0.40       | 0.50  |
| C        | 0.12                     | 0.15       | 0.20  |
| D        | 2.70                     | 2.90       | 3.10  |
| E        | 1.50                     | 1.60       | 1.70  |
| e        | -----                    | 1.90(Typ.) | ----- |
| H        | 2.6                      | 2.8        | 3.00  |
| L        | 0.37                     | -----      | ----- |
| $\theta$ | 14                       | 5          | 9     |