1.5MHZ,600mA,High Efficiency Synchronous PWM Step-Down DC/DC Convert

General Description

The LP3203 is a constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency. The 2.1V to 5.5V input voltage range makes the LP3203 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy-terminals. Internal synchronous rectifier with low RDS(ON) dramatically reduces conduction loss at PWM mode. The internal synchronous switch increases efficiency while eliminate the need for an external Schottky diode.The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small TSOT-23-5 package provide small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection。

Ordering Information

LP3203 - □□ □□ □

F: Pb-Free

Package Type
J5: TSOT23-5

Output Voltage Type
A: Adjustable type
12: 1.2V
15: 1.5V
18: 1.8V
25: 2.5V
33: 3.3V

Features

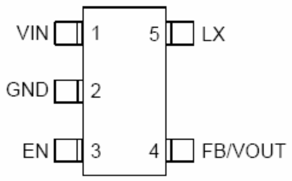
- High Efficiency: 93%
- 1.5MHz Fixed-Frequency PWM Operation
- Adjustable Output From 0.6V to VIN
- 1.2V, 1.5V, 1.8V, 2.5V, 2.8V and 3.3V Fixed
- 600mA Output Current, 1.1A Peak Current
- No Schottky Diode Required
- 100% Duty Cycle Low Dropout Operation
- Available in TSOT23-5 Package
- Short Circuit and Thermal Protection
- Over Voltage Protection
- Low than 1μA Shutdown Current

Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- PDA
- DSC
- Wireless Card

Pin Configurations

(TOP VIEW)



SOT-23-5/TSOT-23-5

Marking Information

Please see website.

Typical Application Circuit

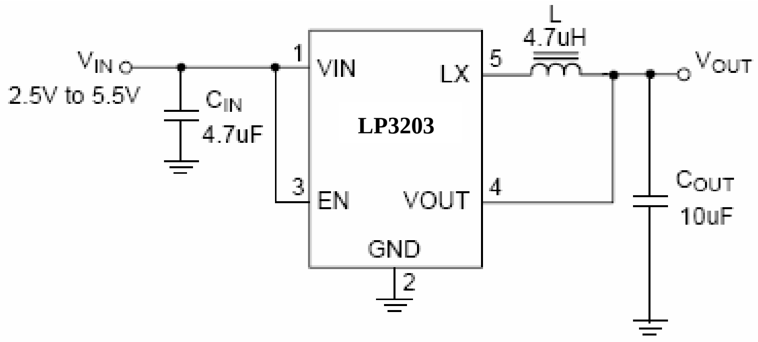
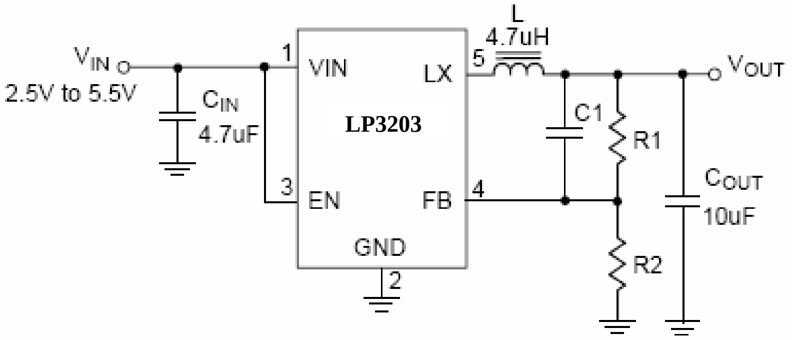


Figure 1. Fixed Voltage Regulator



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with $R1 + R2 \leq 1M\Omega$ and

$V_{REF(Typ.)}$=0.6V

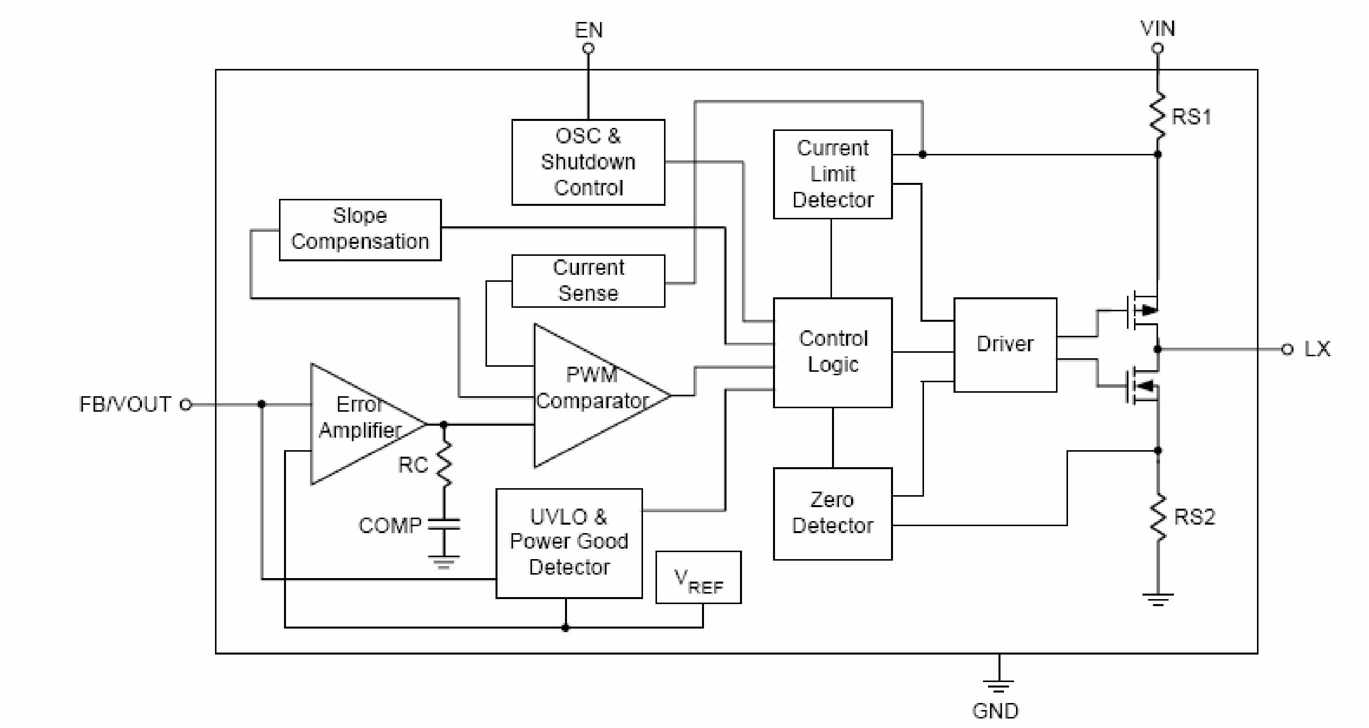
Figure 2. Adjustable Voltage Regulator

MURATA LQH32CN2R2M33
TAIYO YUDEN JMK212BJ475MG
TAIYO YUDEN JAK316BJ106ML

Functional Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Power Input
2	GND	Ground.
3	EN	Chip Enable(Active High).
4	FB/Vout	Feedback Input Pin,Reference voltage is 0.6 V
5	LX	Pin For Switching

Function Block Diagram



Absolute Maximum Ratings

Input Supply Voltage	-0.3V to 6V
EN,VFB Voltage	-0.3V to V_{in}
P-Channel Switch Source Current(DC)	800mA
N-Channel Switch Current(DC)	800mA
Peak SW Sink and Source Current	1.4A
Operation Temperature Range	--40℃ to 85℃
Junction Temperature	125℃
Storage Temperture	--65℃ to 150℃
Lead Temp(Soldering,10sec)	260℃
ESD Rating(HBM)	2KV

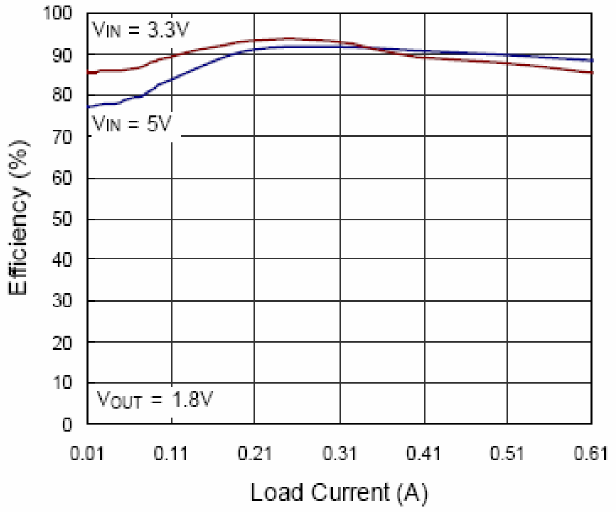
Electrical Characteristics

(VIN = 3.6V, VOUT = 2.5V, VREF = 0.6V, L = 2.2μH, CIN= 4.7μF, COUT= 10μF, TA= 25°C, IMAX = 600mA unless otherwise specified)

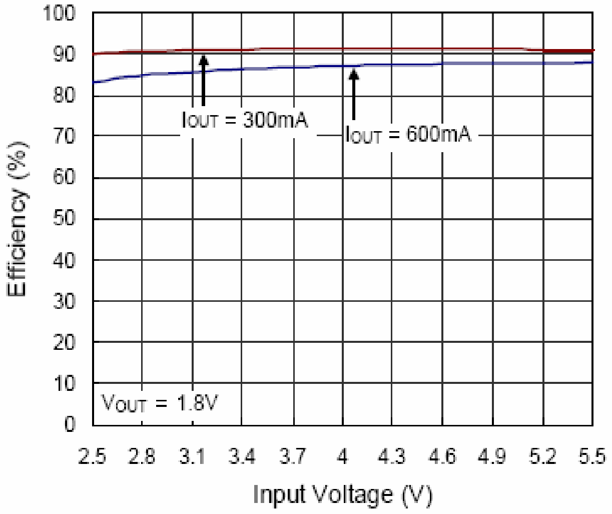
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range		VIN		2.5		5.5	V
Quiescent Current		IQ	IOUT = 0mA, VFB = VREF + 5%		150	200	uA
Shutdown Current		ISHDN	EN = GND		0.1	1	uA
Reference Voltage		VREF	For adjustable output voltage	0.58	0.6	0.62	V
Adjustable Output Range		VOUT		VREF		VIN − 0.2	V
Output Voltage Accuracy	Fixed	ΔVOUT	VIN = 2.2 to 5.5V, VOUT = 1.2V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 2.2 to 5.5V, VOUT = 1.5V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 2.2 to 5.5V, VOUT = 1.8V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 2.8 to 5.5V, VOUT = 2.5V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = 3.5 to 5.5V, VOUT = 3.3V 0A < IOUT < 600mA	−3		+3	%
	Adjustable	ΔVOUT	VIN = VOUT + 0.2V to 5.5V, VIN ≧ 3.5V 0A < IOUT < 600mA	−3		+3	%
		ΔVOUT	VIN = VOUT + 0.4V to 5.5V, VIN ≧ 2.2V 0A < IOUT < 600mA	−3		+3	%
FB Input Current	IFB	VFB = VIN		-30		30	nA
PMOSFET RON	PRDS(ON)	IOUT = 200mA	VIN = 3.6V		0.4	0.58	Ω
NMOSFET RON	NRDS(ON)	IOUT = 200mA	VIN = 3.6V		0.35		Ω
P-Channel Current Limit	IP(LM)	VIN =2.2 to 5.5V		0.9	1	1.5	A
EN Threshold	VEN			0.4		1.5	V
EN Leakage Current	VENL			--	2		uA

Typical Operating Characteristics

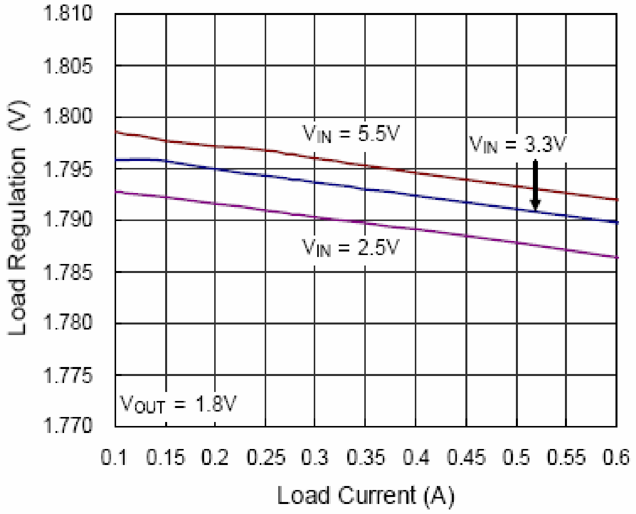
Efficiency vs. Load Current



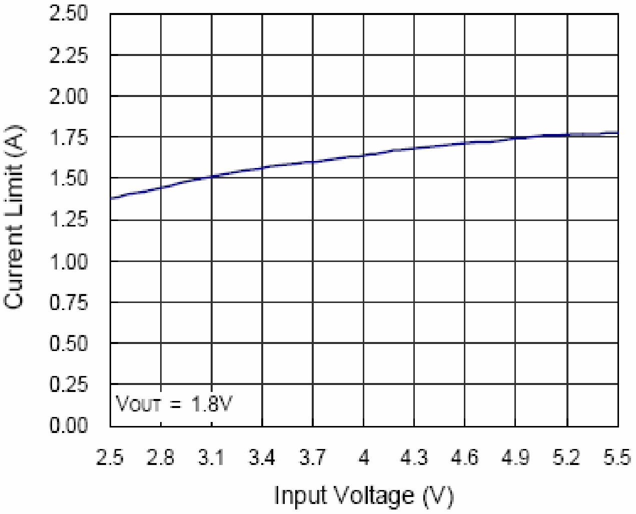
Efficiency vs. Input Voltage



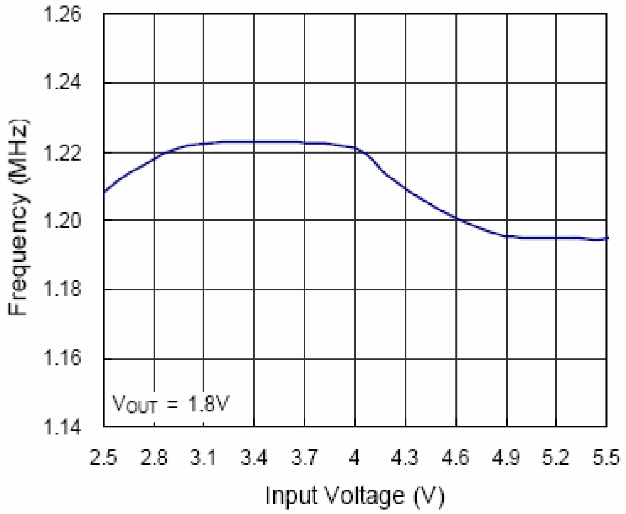
Load Regulation



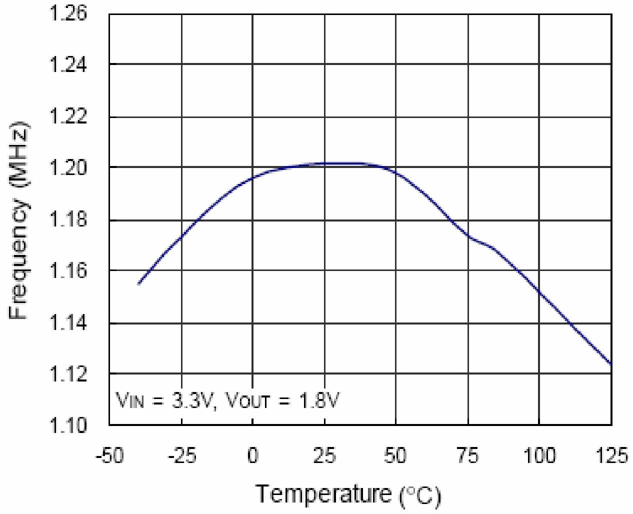
Current Limit vs. Input Voltage



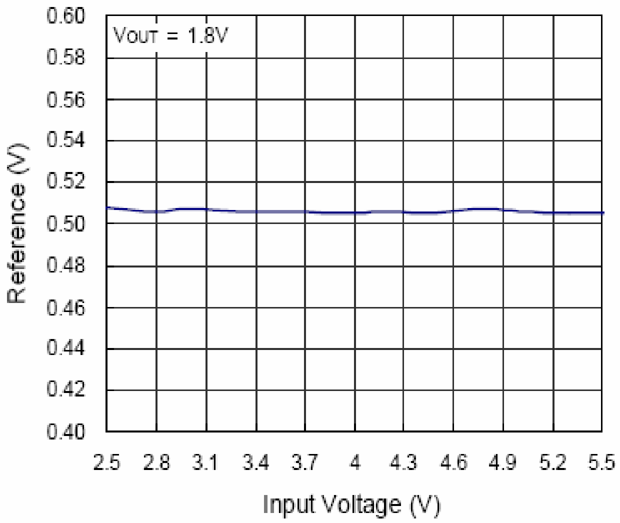
Frequency vs. Input Voltage



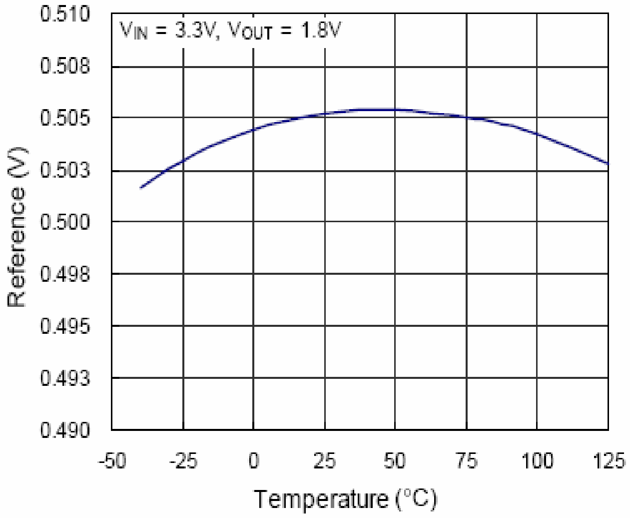
Frequency vs. Temperature



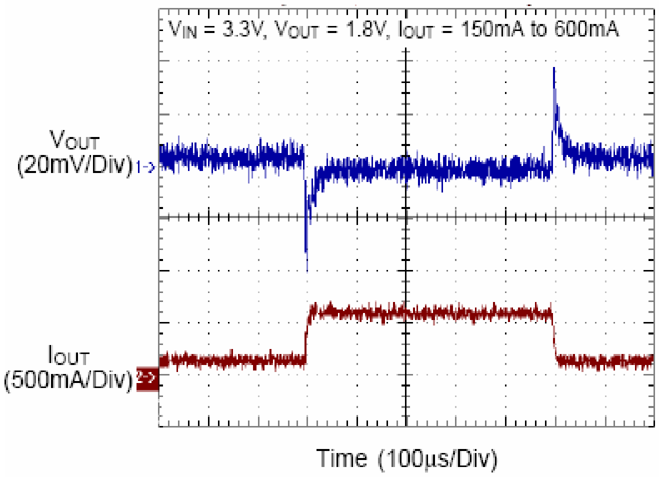
Reference vs. Input Voltage



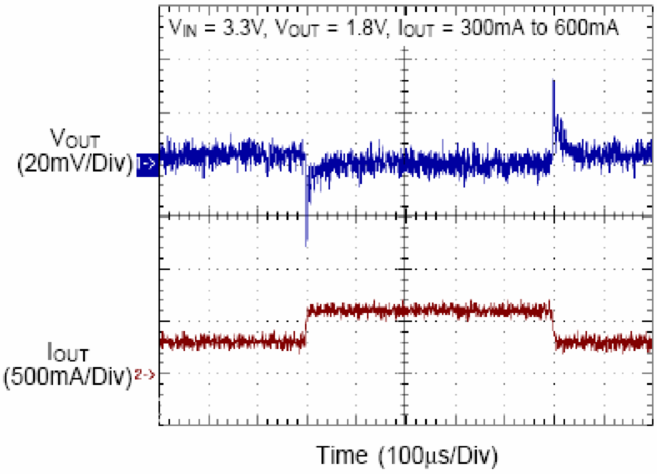
Reference vs. Temperature



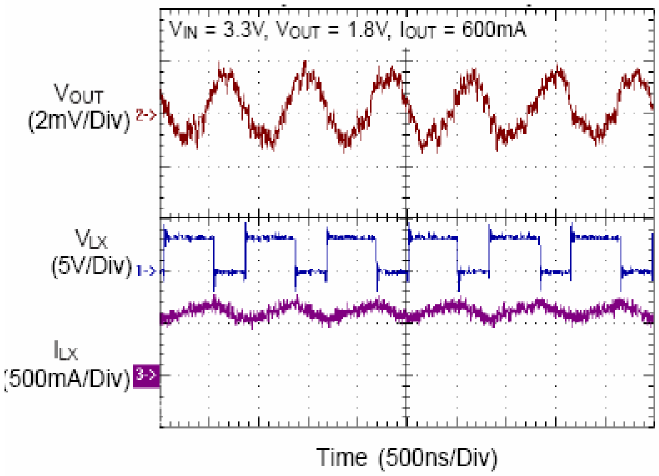
Load Transient Response



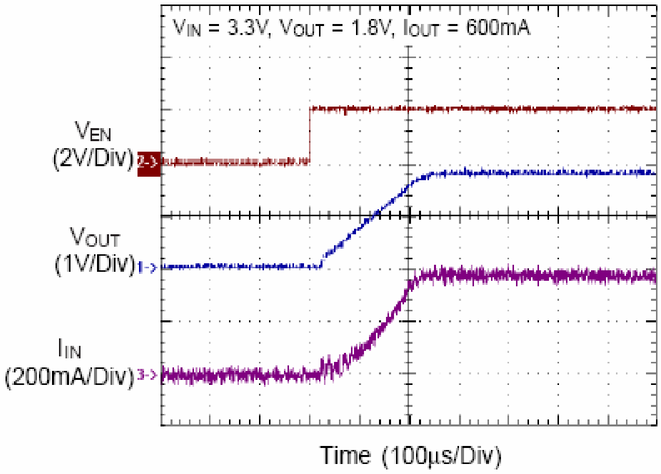
Load Transient Response



Output Ripple



Power On



Applications Information

The basic LP3203 applicaton circuit is shown inTypical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by CIN and COUT.

Inductor selection

The output inductor is selected to limit the ripple current to some predetermined value. typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher Vin or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is $\triangle I_L$=240mA(40% of 600mA).

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right]\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated Inductor should be enough for most applications (600mA+120mA). For better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN} ,is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor Sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$, where $I_{RMS}=I_{OUT}/2$.this simple worst-case condition is commonly.Used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the Capacitor, or choose a capacitor rated at a higher temperature Than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance(ESR) that is required to minimize voltage ripple and load step transients, an well as the amount or bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viesing the load transient response as described in later section.the output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

Using ceramic input and output capacitors

Higher values, lower cost ceramic capacitors are now becoming .Available in smaller case sizes ,their high ripple current ,high voltage rating and low ESR make them ideal for switching regulator applications. however care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is use at input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input ,V_{IN}, At worst,a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

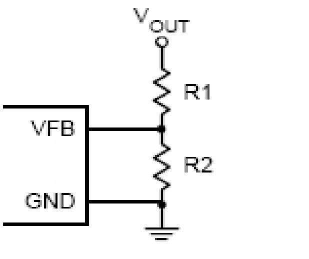
Output voltage programming

The output voltage is set by a resistive divider according to the

Following formula:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right)$$

The external resistive divider is connected to the output, allowing Remote voltage sensing as shown in figure3.



Efficiency considerations

The efficiency of a switching regulator is equal to the output Power divided by the input power times 100%.it is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement efficiency can be expressed as :

Efficiency= 100%- (L1+L2+L3…)

Where L1、L2, etc. are the individual losses as a percentage of Input power .although all dissipative elements in the for most of losses: VIN quiescent current and 1^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1.The VIN quiescent current is due to two components: the DC Bias current as given in the electrical characteristics and the Internal main switch and synchronous switch gate charge currents. the gate charge current results from switching the gate capacitance of the internal power MOSFET switches .Each time the gate charge current. results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switches from high to low to high again, a packet of charge △Q moves from V_{IN} to ground.

The resulting △Q/△t is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode.

$$L_{GATCHG}=f(Q_T+Q_B)$$

Where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. 1^2Rlosses tae calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. in continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFER $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1–DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETS can be obtained from the typical performance characteristics curves. thus, to obtain 1^2R losses, simply add R_{SW} to R_L and multiply the square of the average output current.

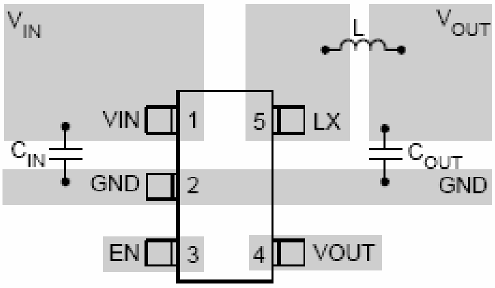
Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

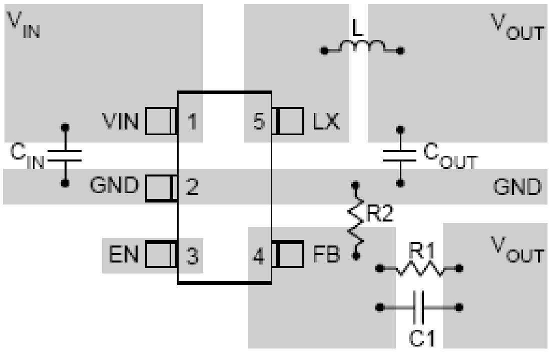
Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to ∆ILOAD (ESR), where ESR is the effective series resistance of COUT. ∆ILOAD also begins to charge or discharge COUT generating a feedback error signal used by the regulator to return VOUT to its steady-state value. During this recovery time, VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

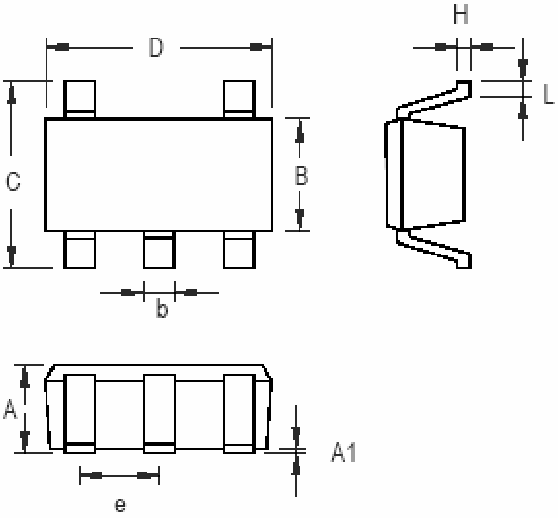
- Follow the PCB layout guidelines for optimal performance of LP3203.
- For the main current paths as indicated in bold lines, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the LP3203.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.





Packaging Information

TSOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package