

LPM9013

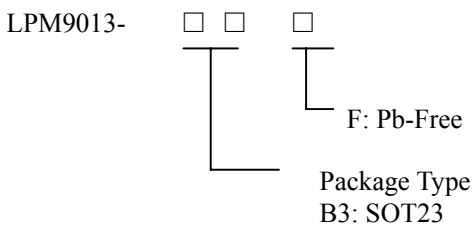
P-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM9013 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Ordering Information



Features

- -20V/-2.6A, $R_{DC(ON)}=125m\Omega$ (typ.)@ $V_{GS}=-2.5V$
- -20V/-3.0A, $R_{DC(ON)}=98m\Omega$ (typ.)@ $V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DC(ON)}$
- SOT23 Package

Applications

- ✧ Portable Media Players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

Marking Information

Please see website.

Pin Configurations



Functional Pin Description

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V_{DS}	-20	V	
Gate-Source Voltage		V_{GS}	± 8	V	
Continuous Drain Current ^A	$T_A=25^\circ\text{C}$	I_D	-3	A	
	$T_A=70^\circ\text{C}$		-2.4		
Pulsed Drain Current ^B			I_{DM}		
Power Dissipation ^A	$T_A=25^\circ\text{C}$	P_D	1.4	W	
	$T_A=70^\circ\text{C}$		0.9		
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	70	90	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	Steady-State		100	125	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	63	80	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-16V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±8V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-0.3	-0.55	-1	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-15			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-3A T _J =125°C		81 111	97 135	mΩ
		V _{GS} =-2.5V, I _D =-2.6A		108	130	mΩ
		V _{GS} =-1.8V, I _D =-1A		146	190	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	4	7		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.78	-1	V
I _S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			540		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		72		pF
C _{rss}	Reverse Transfer Capacitance			49		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		12		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge			6.1		nC
Q _{gs}	Gate Source Charge	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-3A		0.6		nC
Q _{gd}	Gate Drain Charge			1.6		nC
t _{D(on)}	Turn-On DelayTime			10		ns
t _r	Turn-On Rise Time	V _{GS} =-4.5V, V _{DS} =-10V, R _L =3.3Ω, R _{GEN} =3Ω		12		ns
t _{D(off)}	Turn-Off DelayTime			44		ns
t _f	Turn-Off Fall Time			22		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-3A, dI/dt=100A/μs		21		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-3A, dI/dt=100A/μs		7.5		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t_s 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

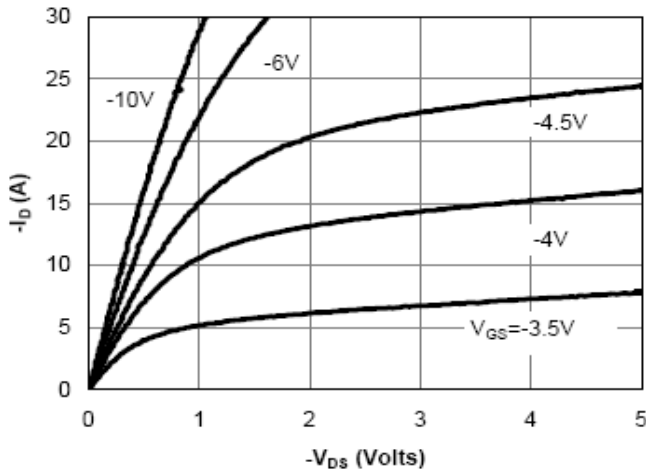


Fig 1: On-Region Characteristics (Note E)

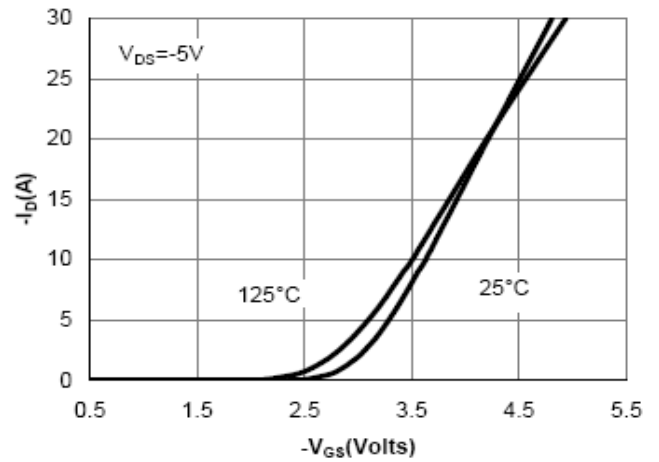


Figure 2: Transfer Characteristics (Note E)

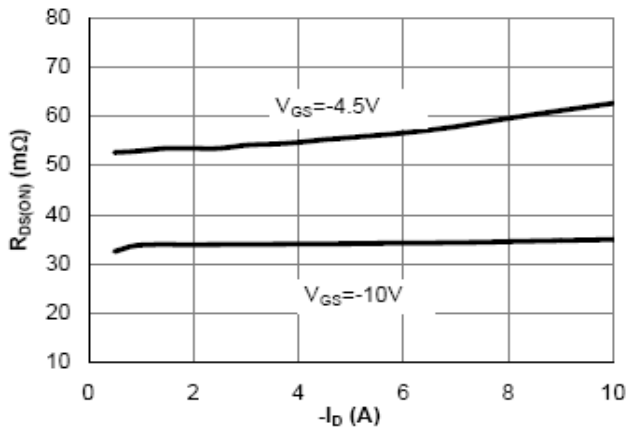


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

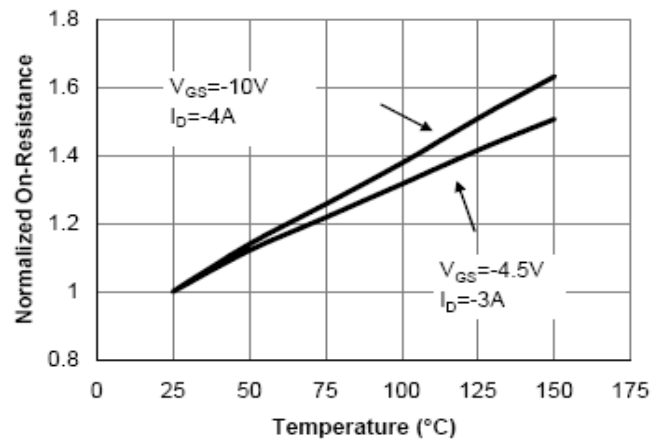


Figure 4: On-Resistance vs. Junction Temperature (Note E)

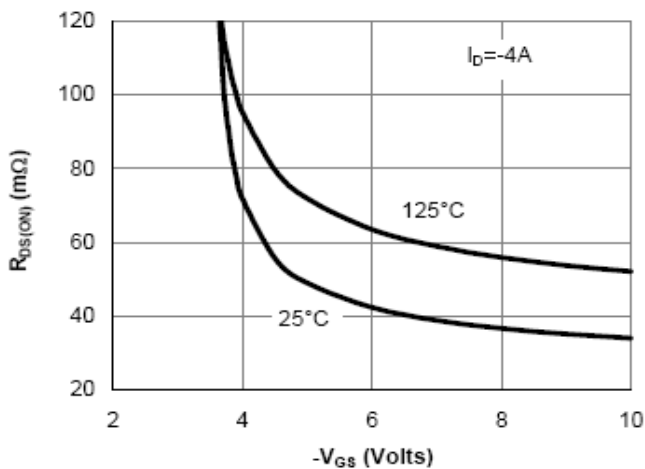


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

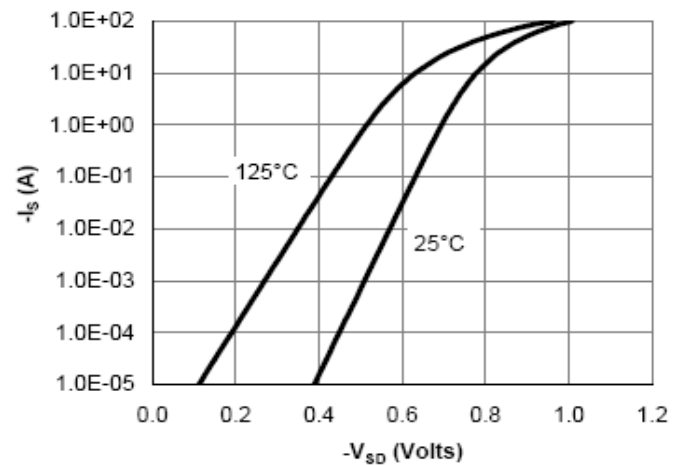


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

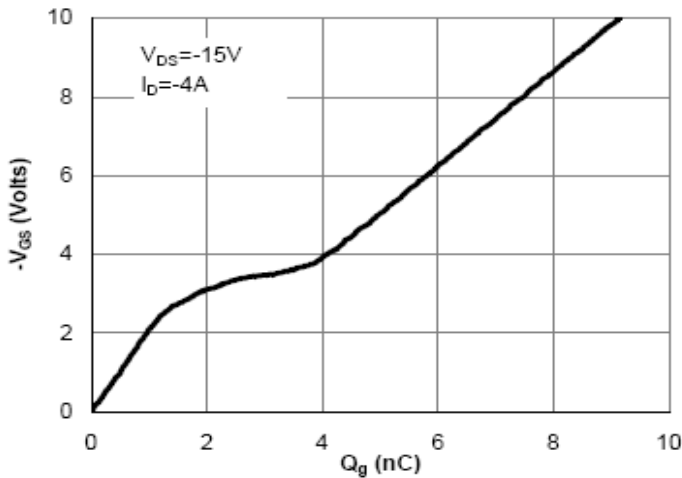


Figure 7: Gate-Charge Characteristics

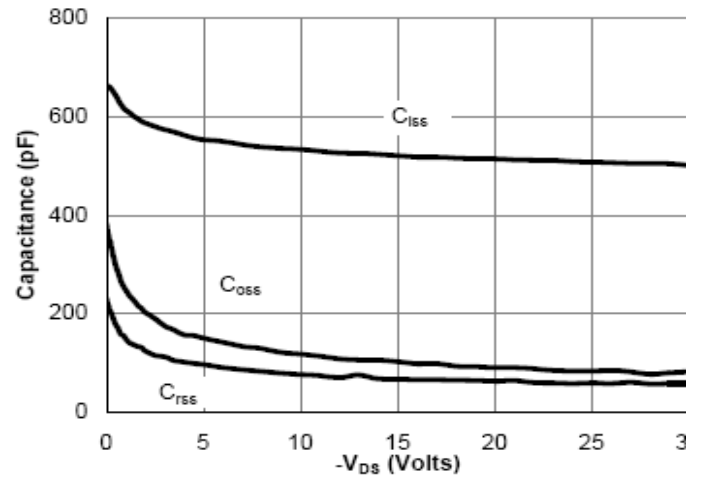


Figure 8: Capacitance Characteristics

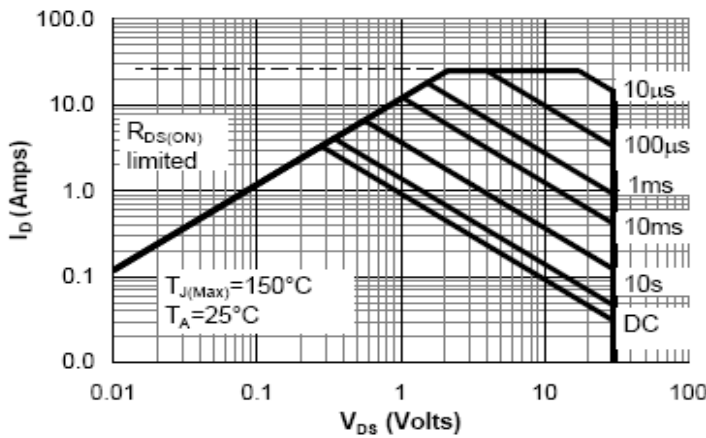


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

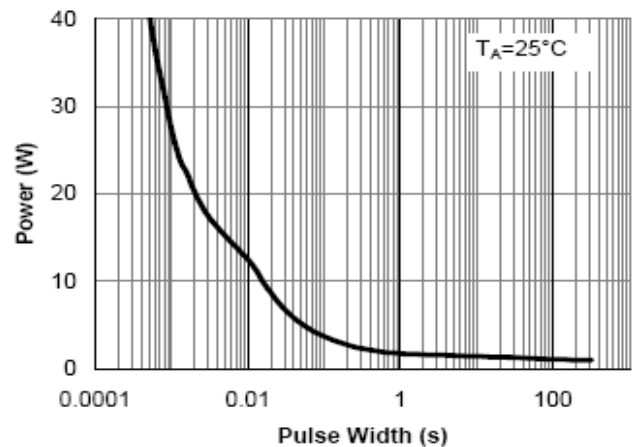


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

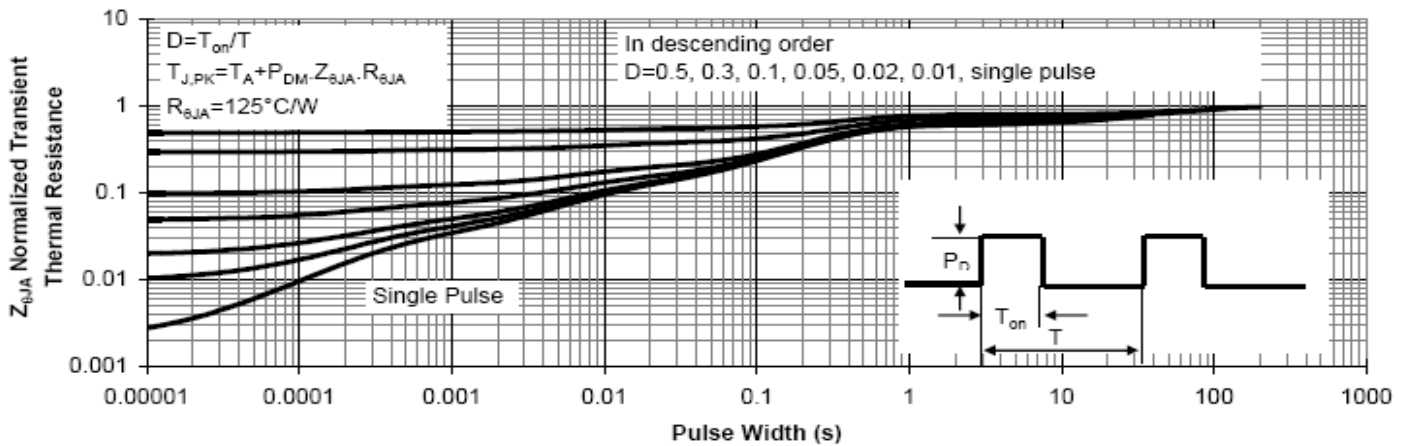
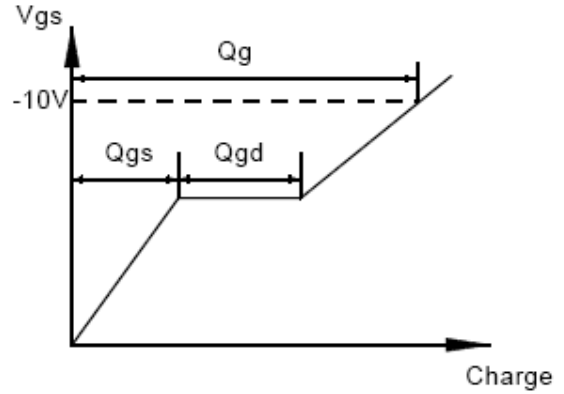
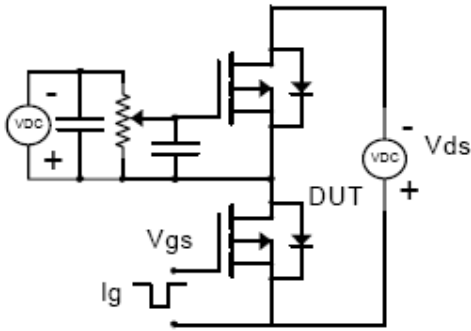
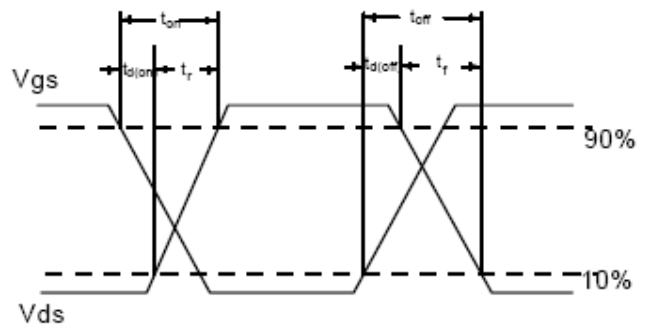
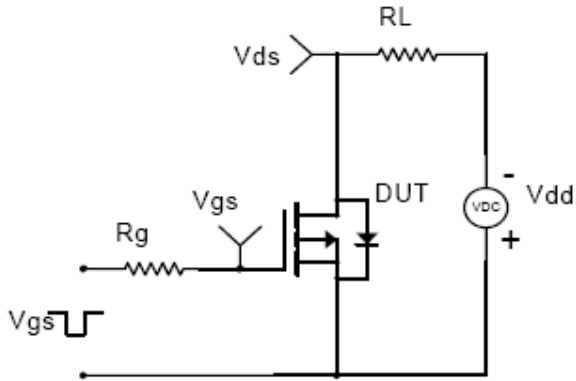


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

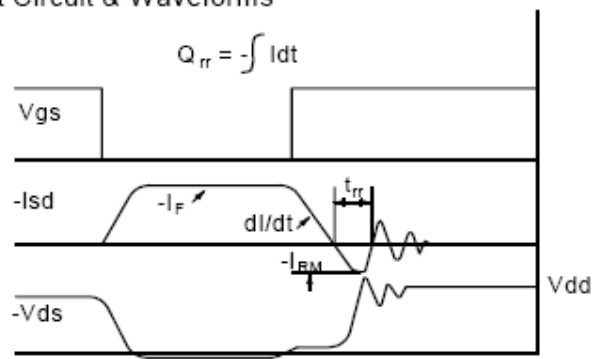
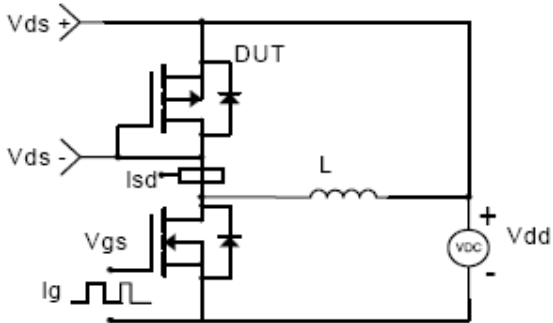
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

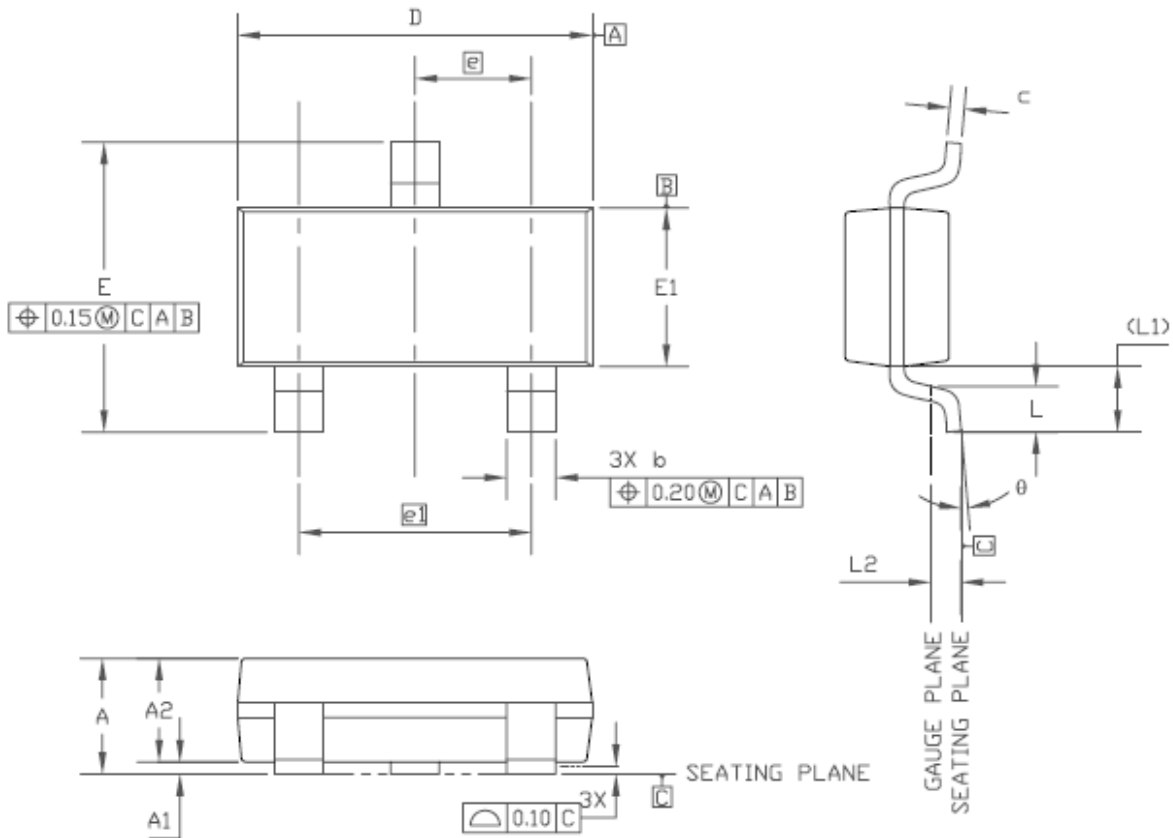


Diode Recovery Test Circuit & Waveforms

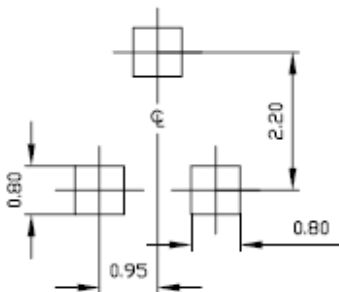


Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°